CHARGEUR DE BATTERIE POUR VEHICULE ELECTRIQUE

DOCUMENTATION TECHNIQUE

FAIRCHILD
SEMICONDUCTOR®

HIGH SPEED-10 MBit/s LOGIC GATE OPTOCOUPLERS

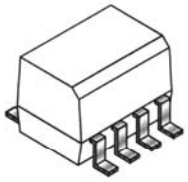
HCPL-0600 HCPL-0601

DESCRIPTION

The HCPL-0600/0601optocouplers consist of a 870 nm AlGaAS LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. The devices are housed in a compact small-outline package. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8). An internal noise shield provides superior common mode rejection of typically 10 kV/µs.

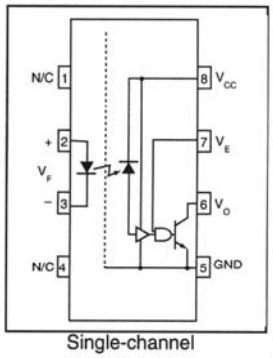
FEATURES

- Compact SO8 package
- Very high speed-10 MBit/s
- Superior CMR-10 kV/µs
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700)



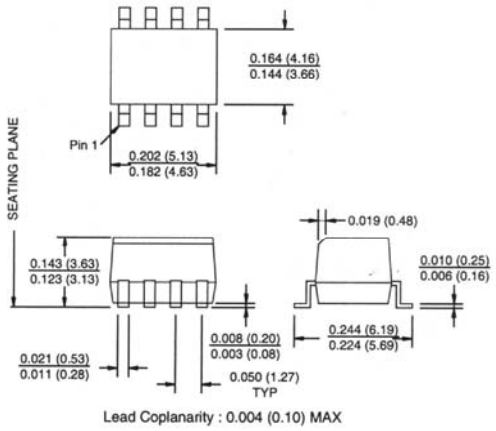
APPLICATIONS

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface



Single-channel circuit drawing

PACKAGE DIMENSIONS



NOTE
All dimensions are in inches (millimeters)

TRUTH TABLE (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

A 0.1 µF bypass capacitor must be connected between pins 8 and 5. (See note 1)

8/27/02

FAIRCHILD SEMICONDUCTOR®

HIGH SPEED-10 MBit/s LOGIC GATE OPTOCOUPLERS

HCPL-0600 HCPL-0601

ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C Unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit
EMITTER	(I_F = 10 mA)	V_F			1.8	V
Input Forward Voltage	T_A =25°C				1.75	
Input Reverse Breakdown Voltage	(I_R = 10 µA)	B_{VR}	5.0			V
Input Capacitance	(V_F = 0, f = 1 MHz)	C_{IN}		60		pF
Input Diode Temperature Coefficient	(I_F = 10 mA)	ΔVF/ΔTA		-1.4		mV/°C
DETECTOR						
High Level Supply Current	(V_{CC} = 5.5 V, I_F = 0 mA) (V_E = 0.5 V)	I_{CCH}		7	10	mA
Low Level Supply Current	(V_{CC} = 5.5 V, I_F = 10 mA) (V_E = 0.5 V)	I_{CCL}		9	13	mA
Low Level Enable Current	(V_{CC} = 5.5 V, V_E = 0.5 V)	I_{EL}		-0.8	-1.6	mA
High Level Enable Current	(V_{CC} = 5.5 V, V_E = 2.0 V)	I_{EH}		-0.6	-1.6	mA
High Level Enable Voltage	(V_{CC} = 5.5 V, I_F = 10 mA)	V_{EH}	2.0			V
Low Level Enable Voltage	(V_{CC} = 5.5 V, I_F = 10 mA) (Note 2)	V_{EL}			0.8	V

SWITCHING CHARACTERISTICS (T_A = -40°C to +85°C, V_{CC} = 5 V, I_F = 7.5 mA Unless otherwise specified.)

AC Characteristics	Test Conditions		Device	Symbol	Min	Typ	Max	Unit
Propagation Delay Time to Output High Level	(Note 3)	(T_A =25°C)	All	T_{PLH}	20	45	75	ns
	(R_L = 350Ω, C_L = 15 pF) (Fig. 12)						100	
Propagation Delay Time to Output Low Level	(Note 4)	(T_A =25°C)	All	T_{PHL}	25	45	75	ns
	(R_L = 350Ω, C_L = 15 pF) (Fig. 12)					100		
Pulse Width Distortion	(R_L = 350Ω, C_L = 15 pF) (Fig. 12)		All	$\lvert T_{PHL}-T_{PLH}\rvert$		3	35	ns
Output Rise Time (10-90%)	(R_L = 350Ω, C_L = 15 pF) (Note 5) (Fig. 12)		All	t_r		50		ns
Output Fall Time (90-10%)	(R_L = 350Ω, C_L = 15 pF) (Note 6) (Fig. 12)		All	t_f		12		ns
Enable Propagation Delay Time to Output High Level	(I_F = 7.5 mA, V_{EH} = 3.5 V) (R_L = 350Ω, C_L = 15 pF) (Note 7) (Fig. 13)		All	t_{ELH}		20		ns
Enable Propagation Delay Time to Output Low Level	(I_F = 7.5 mA, V_{EH} = 3.5 V) (R_L = 350Ω, C_L = 15 pF) (Note 8) (Fig. 13)		All	t_{EHL}		20		ns
Common Mode Transient Immunity (at Output High Level)	(R_L = 350Ω) (T_A =25°C) (I_F = 0 mA, V_{OH} (Min.) = 2.0 V) (Note 9)(Fig. 14)	$\lvert V_{CM}\rvert$ = 10 V	HCPL-0600	$\lvert CM_H\rvert$		10,000		V/µs
		$\lvert V_{CM}\rvert$ = 50 V	HCPL-0601		5000	10,000		
Common Mode Transient Immunity (at Output Low Level)	(R_L = 350Ω) (T_A =25°C) (I_F = 7.5 mA, V_{OL} (Max.) = 0.8 V) (Note 10)(Fig. 14)	$\lvert V_{CM}\rvert$ = 10 V	HCPL-0600	$\lvert CM_H\rvert$		10,000		V/µs
		$\lvert V_{CM}\rvert$ = 50 V	HCPL-0601		5000	10,000		

August 2000

National Semiconductor

LMC662
CMOS Dual Operational Amplifier

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

Features

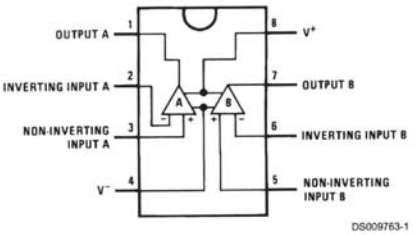
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain: 126 dB
- Low input offset voltage: 3 mV
- Low offset voltage drift: 1.3 µV/°C
- Ultra low input bias current: 2 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- I_{SS} = 400 µA/amplifier; independent of V+
- Low distortion: 0.01% at 10 kHz
- Slew rate: 1.1 V/µs
- Available in extended temperature range (−40°C to +125°C); ideal for automotive applications
- Available to a Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram

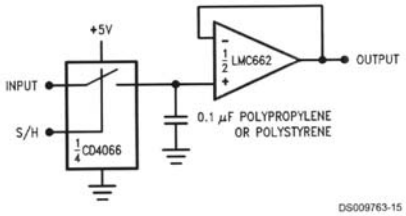
8-Pin DIP/SO



DS009763-1

Typical Application

Low-Leakage Sample-and-Hold



DS009763-15

PALCE16V8 COM'L:H-5/7/10/15/25, Q-10/15/25 IND:H-10/25, Q-20/25
PALCE16V8Z COM'L:-25 IND:-12/15/25

VANTIS
BEYOND PERFORMANCE

PALCE16V8 and PALCE16V8Z Families

EE CMOS (Zero-Power) 20-Pin Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- **Pin and function compatible with all 20-pin PAL® devices**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - — 5-ns propagation delay for "-5" version
  - — 7.5-ns propagation delay for "-7" version
- **Direct plug-in replacement for the PAL16R8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Peripheral Component Interconnect (PCI) compliant**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support**
- **Fully tested for 100% programming and functional yields and high reliability**
- **5-ns version utilizes a split leadframe for improved performance**

GENERAL DESCRIPTION

The PALCE16V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8, with the exception of the PAL16C1.

The PALCE16V8Z provides zero standby power and high speed. At 30-µA maximum standby current, the PALCE16V8Z allows battery-powered operation for an extended period.

The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

Publication# 16493 Rev: E
Amendment/0 Issue Date: November 1998

DALLAS SEMICONDUCTOR

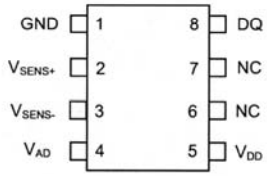
DS2438
Smart Battery Monitor

www.maxim-ic.com

FEATURES

- Unique 1-Wire® interface requires only one port pin for communication
- Provides unique 64-bit serial number to battery packs
- Eliminates thermistors by sensing battery temperature on-chip
- On-board A/D converter allows monitoring of battery voltage for end-of-charge and end-of-discharge determination
- On-board integrated current accumulator facilitates fuel gauging
- Elapsed time meter in binary format
- 40-byte nonvolatile user memory available for storage of battery-specific data
- Operating range -40°C to +85°C
- Applications include portable computers, portable/cellular phones, consumer electronics, and handheld instrumentation

PIN ASSIGNMENT



DS2438Z, DS2438AZ
8-Pin SOIC (150-mil)

PIN DESCRIPTION

DQ	-	Data In/Out
VAD	-	General A/D input
V_{SENS+}	-	Battery current monitor input (+)
V_{SENS-}	-	Battery current monitor input (-)
VDD	-	Power Supply (2.4V to 10.0V)
GND	-	Ground
NC	-	No connect

DESCRIPTION

The DS2438 Smart Battery Monitor provides several functions that are desirable to carry in a battery pack: a means of tagging a battery pack with a unique serial number, a direct-to-digital temperature sensor which eliminates the need for thermistors in the battery pack, an A/D converter which measures the battery voltage and current, an integrated current accumulator which keeps a running total of all current going into and out of the battery, an elapsed time meter, and 40 bytes of nonvolatile EEPROM memory for storage of important parameters such as battery chemistry, battery capacity, charging methodology and assembly date. Information is sent to/from the DS2438 over a 1-Wire interface, so that only one wire (and ground) needs to be connected from a central microprocessor to a DS2438. This means that battery packs need only have three output connectors: battery power, ground, and the 1-Wire interface.

Because each DS2438 contains a unique silicon serial number, multiple DS2438s can exist on the same 1-Wire bus. This allows multiple battery packs to be charged or used in the system simultaneously.

Applications for the smart battery monitor include portable computers, portable/cellular telephones, and handheld instrumentation battery packs in which it is critical to monitor real-time battery performance. Used in conjunction with a microcontroller in the host system, the DS2438 provides a complete smart battery pack solution that is fully chemistry-independent. The customization for a particular battery chemistry and capacity is realized in the code programmed into the microcontroller and DS2438 EEPROM, and only a software revision is necessary should a designer wish to change battery pack chemistry.

080602

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	**Ground**
2	V_{SENS+}	**Battery Input:** connection for battery current to be monitored (see text)
3	V_{SENS-}	**Battery Input:** connection for battery current to be monitored (see text)
4	V_{AD}	**ADC Input:** input for general purpose A/D
5	V_{DD}	**V_{DD} Pin:** input supply voltage
6, 7	NC	**No Connect**
8	DQ	**Data Input/Out:** for 1-Wire operation: Open drain

OVERVIEW

The block diagram of Figure 1 shows the seven major components of the DS2438:

1. 64-bit lasered ROM
2. temperature sensor
3. battery voltage A/D
4. battery current A/D
5. current accumulators
6. elapsed time meter
7. 40-byte nonvolatile user-memory

Each DS2438 contains a unique 64-bit lasered ROM serial number so that several battery packs can be charged/monitored by the same host system. Furthermore, other Dallas products featuring the same 1-Wire bus architecture with a 64-bit ROM can reside on the same bus; refer to the Dallas Automatic Identification Data book for the specifications of these products.

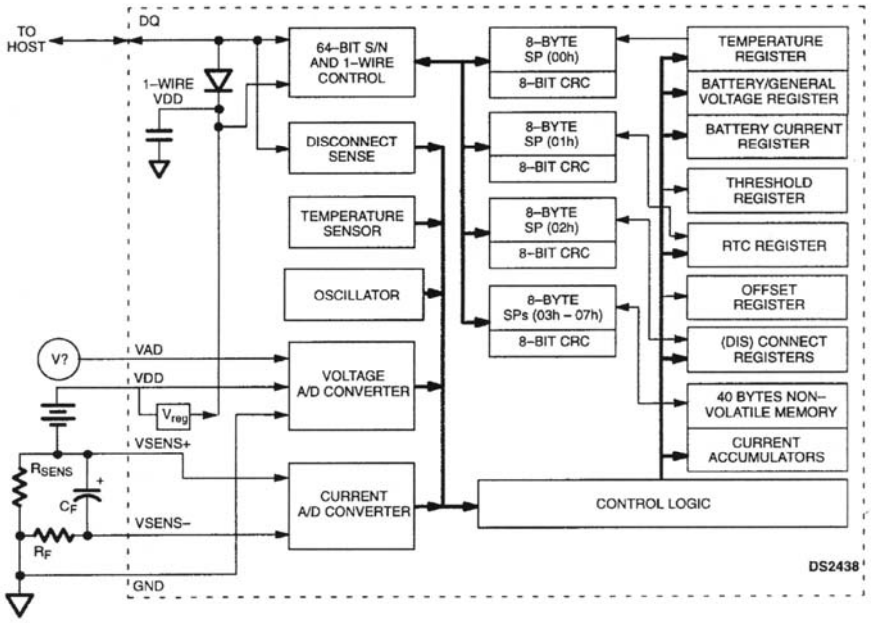
Communication to the DS2438 is via a 1-Wire port. With the 1-Wire port, the memory and control functions will not be available until the ROM function protocol has been established. The master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. These commands operate on the 64-bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1-Wire line as well as to indicate to the bus master how many and what types of devices are present. After a ROM function sequence has been successfully executed, the memory and control functions are accessible and the master may then provide any one of the six memory and control function commands.

Control function commands may be issued which instruct the DS2438 to perform a temperature measurement or battery voltage A/D conversion. The result of these measurements will be placed in the DS2438's memory map, and may be read by issuing a memory function command which reads the contents of the temperature and voltage registers. Additionally, the charging/discharging battery current is measured without user intervention, and again, the last completed result is stored in DS2438 memory space. The DS2438 uses these current measurements to update three current accumulators; the first stores net charge for fuel gauge calculations, the second accumulates the total charging current over the life of the battery, and the remaining accumulator tallies battery discharge current. The elapsed time meter data, which can be used in calculating battery self-discharge or time-related charge termination limits, also resides in the DS2438 memory map and can be extracted with a memory function command. The nonvolatile user memory of the DS2438 consists of 40 bytes of EEPROM. These locations may be used to store any data the user wishes and are written to using a memory function command. All data and commands are read and written least significant bit first.

PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the DQ pin is high. DQ will provide sufficient power as long as the specified timing and voltage requirements are met (see the section titled "1-Wire Bus System"). The advantage of parasite power is that the ROM may be read in absence of normal power, i.e., if the battery pack is completely discharged.

DS2438 BLOCK DIAGRAM Figure 1



OPERATION-MEASURING TEMPERATURE

The DS2438 measures temperatures through the use of an on-board temperature measurement technique.

The temperature reading is provided in a 13-bit, two's complement format, which provides 0.03125°C of resolution. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 1-Wire interface. The DS2438 can measure temperature over the range of -55°C to +125°C in 0.03125°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Note that temperature is represented in the DS2438 in terms of a 0.03125°C LSb, yielding the following 13-bit format. The 3 least significant bits of the Temperature Register will always be 0. The remaining 13 bits contain the two's complement representation of the temperature in °C, with the MSb holding the sign (S) bit. See "Memory Map" section for the Temperature Register address location.

Temperature Register Format Table 1

2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	0	0	0	LSB
MSb				(unit = °C)			LSb	
S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	MSB

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101 00000000	7D00h
+25.0625°C	00011001 00010000	1910h
+0.5°C	00000000 10000000	0080h
0°C	00000000 00000000	0000h
-0.5°C	11111111 10000000	FF80h
-25.0625°C	11100110 11110000	E6F0h
-55°C	11001001 00000000	C900h

OPERATION-MEASURING BATTERY VOLTAGE

The on-board analog-to-digital converter (ADC) has 10 bits of resolution and will perform a conversion when the DS2438 receives a command protocol (Convert V) instructing it to do so. The result of this measurement is placed in the 2-byte Voltage Register. The range for the DS2438 ADC is 0 volt to 10 volt; this range is suitable for NiCd or NiMH battery packs up to six cells, and for lithium ion battery packs of two cells. The full-scale range of the ADC is scaled to 10.23 volt, resulting in a resolution of 10 mV.

While the ADC has a range that extends down to 0 volt, it is important to note that the battery voltage can also be the supply voltage to the DS2438. As such, the accuracy of the ADC begins to degrade below battery voltages of 2.4 volt, and the ability to make conversions is limited by the operating voltage range of the DS2438.

Voltage is expressed in this register in scaled binary format, as outlined in Table 2. Note that while codes exist for values below 2.4 volt, accuracy of the ADC and the limitation on the DS2438's supply voltage make it unlikely that these values would be used in actual practice. See "Memory Map" section for the Voltage Register address location.

VOLTAGE REGISTER FORMAT Table 2

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB
MSb			(unit = 10 mV)				LSb	
0	0	0	0	0	0	2^9	2^8	MSB

BATTERY VOLTAGE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
0.05V	0000 0000 0000 0101	0005h
2.7V	0000 0001 0000 1110	010Eh
3.6V	0000 0001 0110 1000	0168h
5V	0000 0001 1111 0100	01F4h
7.2V	0000 0010 1101 0000	02D0h
9.99V	0000 0011 1110 0111	03E7h
10V	0000 0011 1110 1000	03E8H

For applications requiring a general purpose voltage A/D converter, the DS2438 can be configured so that the result of a Convert V command will place the scaled binary representation of the voltage on the V_{AD} input (as opposed to the V_{DD} input) into the Voltage Register in the same format described in Table 2. Depending upon the state of the Status/Configuration Register, either (but not both) the V_{DD} or V_{AD} voltage will be stored in the Voltage Register upon receipt of the Convert V command. Refer to the description of the Status/Configuration Register in the Memory Map section for details. If the V_{AD} input is used as the voltage input, the A/D will be accurate for $1.5V < V_{AD} < 2V_{DD}$ over the range $2.4V < V_{DD} < 5.0V$. This feature gives the user the ability to have a voltage A/D that meets spec accuracy for inputs over the entire range of $1.5V < V_{AD} < 10V$ for $V_{DD} = 5.0V$.

OPERATION - MEASURING BATTERY CURRENT

The DS2438 features an A/D converter that effectively measures the current flow into and out of the battery pack by measuring the voltage across an external sense resistor. It does so in the background at a rate of 36.41 measurements/sec; thus, no command is required to initiate current flow measurements. However, the DS2438 will only perform current A/D measurements if the IAD bit is set to "1" in the Status/Configuration Register. The DS2438 measures current flow in and out of the battery through the V_{SENS} pins; the voltage from the V_{SENS+} pin to the V_{SENS-} pin is considered to be the voltage across the current sense resistor, R_{SENS}. The V_{SENS+} terminal may be tied directly to the R_{SENS} resistor, however, for V_{SENS-}, we recommend use of an RC low pass filter between it and the GND end of R_{SENS} (see the block diagram in Figure 1). Using a 100 kΩ (min) resistor (R_F) and a 0.1 µF tantalum capacitor (C_F), the filter cutoff is approximately 15.9 Hz. The current A/D measures at a rate of 36.41 times per second, or once every 27.46 ms. This filter will capture the effect of most current spikes, and will thus allow the current accumulators to accurately reflect the total charge which has gone into or out of the battery.

The voltage across current sense resistor R_{SENS} is measured by the ADC and the result is placed in the Current Register in two's complement format. The sign (S) of the result, indicating charge or discharge, resides in the most significant bit of the Current Register, as shown in Table 3. See "Memory Map" in Figure 7 for the Current Register address location.

CURRENT REGISTER FORMAT Table 3

(This register actually stores the voltage measured across current sense resistor R_{SENS}. This value can be used to calculate battery pack current using the equation below.)

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB
MSb			(unit = 0.2441mV)				LSb	
S	S	S	S	S	S	2^9	2^8	MSB

The battery pack current is calculated from the Current Register value using the equation:

I = Current Register / (4096 * R_{SENS}) (where R_{SENS} is in Ω)

For example, if 1.25A is flowing into the pack, and the pack uses a 0.025Ω sense resistor, the DS2438 will write the value 128_{10} to the Current Register. From this value, battery pack current can be calculated to be:

$I = 128 / (4096 * 0.025) = 1.25A$

Because small current ADC offset errors can have a large cumulative effect when current is integrated over time, the DS2438 provides a method for canceling offset errors in the current ADC. After each current measurement is completed, the measured value is added to the contents of the Offset Register and the result is then stored in the Current Register. The Offset Register is a two-byte nonvolatile read/write register formatted in two's-complement format. The four MSb's of the register contain the sign of the offset, as shown in Table 4.

OFFSET REGISTER FORMAT Table 4

2^4	2^3	2^2	2^1	2^0	0	0	0	LSB
MSb			(unit = 0.2441 mV)				LSb	
X	X	X	S	2^8	2^7	2^6	2^5	MSB

The following process can be used to calibrate the current ADC:

1. Write all zeroes to the Offset Register
2. Force zero current through R_{SENS}
3. Read the Current Register value
4. Disable the current ADC by setting the IAD bit in the Status/Configuration Register to "0"
5. Change the sign of the previously-read Current Register value by performing the two's complement and write the result to the Offset Register
6. Enable the current ADC by setting the IAD bit in the Status/Configuration Register to "1"

NOTE:

When writing to the Offset Register, current measurement MUST be disabled (IAD bit set to "0").

The current ADC calibration process is done for each DS2438 device prior to shipment. However, for best results, battery pack manufacturers should calibrate the current ADC during initial battery pack testing, and the host system should calibrate whenever possible (during battery charging, for example).

OPERATION - CURRENT ACCUMULATORS

The DS2438 tracks the remaining capacity of a battery using the Integrated Current Accumulator (ICA). The ICA maintains a net accumulated total of current flowing into and out of the battery; therefore, the value stored in this register is an indication of the remaining capacity in a battery and may be used in performing fuel gauge functions. In addition, the DS2438 has another register that accumulates only charging (positive) current (CCA) and one that accumulates only discharging (negative) current (DCA). The CCA and DCA give the host system the information needed to determine the end of life of a rechargeable battery, based on total charge/discharge current over its lifetime.

The current measurement described above yields the voltage across sense resistor R_{SENS} measured every 27.46 ms. This value is then used to increment or decrement the ICA register, increment the CCA (if current is positive), or increment the DCA (if current is negative). The ICA is a scaled 8-bit volatile binary counter that integrates the voltage across R_{SENS} over time. The ICA is only incremented/decremented if the IAD bit is set to 1 in the Status/Configuration Register. Table 5 illustrates the contents of the ICA. See Memory Map section for the address location of the ICA.

ICA REGISTER FORMAT Table 5

(This register accumulates the voltage measured across current sense resistor R_{SENS}. This value can be used to calculate remaining battery capacity using the equation below.)

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb (unit = 0.4882 mVhr) LSb

Remaining battery capacity is calculated from the ICA value using the equation:

Remaining Capacity = ICA / (2048 * R_{SENS}) (where R_{SENS} is in Ω)

For example, if a battery pack has 0.625 Ahr of remaining capacity, and the pack uses a 0.025Ω sense resistor, the ICA will contain the value 32. From this value, remaining capacity can be calculated to be:

Remaining Capacity = 32 / (2048 * 0.025) = 0.625 Ahr

Since the accuracy of the current ADC is ±2 LSb, measurements of very small currents can be inaccurate by a high percentage. Because these inaccuracies can turn into large ICA errors when accumulated over a long period of time, the DS2438 provides a method for filtering out potentially erroneous small signals so that they are not accumulated. The DS2438's Threshold Register specifies a current measurement magnitude (after offset cancellation) above which the measurement is accumulated in the ICA, CCA and DCA and below which it is not accumulated. The format of the Threshold Register is shown in Table 6. The power-on default Threshold Register value is 00h (no threshold).

NOTE:

When writing to the Threshold Register, current measurement must be disabled (IAD bit set to "0").

THRESHOLD REGISTER FORMAT Table 6

TH2	TH1	0	0	0	0	0	0

MSb LSb

TH2	TH1	THRESHOLD
0	0	None (default)
0	1	±2 LSB
1	0	±4 LSB
1	1	±8 LSB

The Charging Current Accumulator (CCA) is a two-byte nonvolatile read/write counter which represents the total charging current the battery has encountered in its lifetime. It is only updated when current through R_{SENS}, is positive; i.e., when the battery is being charged. Similarly, the Discharge Current Accumulator (DCA) is a two-byte nonvolatile counter which represents the total discharging current the battery has encountered over its lifetime.

The CCA and DCA can be configured to function in any of three modes: disabled, enabled with shadow-to-EEPROM, and enabled without shadow-to-EEPROM. When the CCA and DCA are disabled (by setting either the IAD bit or the CA bit in the Status/Configuration Register to "0"), the memory in page 07h is free for general purpose data storage. When the CCA and DCA are enabled (by setting both IAD and CA to "1"), page 07h is reserved for these registers, and none of the bytes in page 07h should be written to via the 1-Wire bus. When the CCA and DCA are enabled, their values are automatically shadowed to EEPROM memory by setting the EE bit in the Status/Configuration Register to "1". When these registers are configured to shadow to EEPROM, the information will accumulate over the lifetime of the battery pack and will not be lost when the battery becomes discharged. Shadow-to-EEPROM is disabled when the EE bit is "0". Table 7 illustrates the format of the CCA and DCA registers. Table 8 summarizes the modes of operation for ICA, CCA and DCA.

CCA/DCA REGISTER FORMAT Table 7

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB

MSb (unit = 15.625 mVHr) LSb

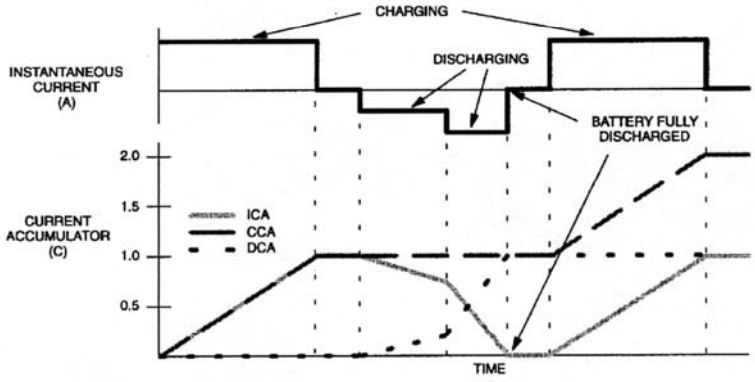
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	MSB

ICA/CCA/DCA MODES OF OPERATION Table 8

IAD Bit	CA Bit	EE Bit	ICA	CCA/DCA	CCA/DCA Copy-to-EEPROM
0	X	X	Inactive	Inactive	Inactive
1	0	X	Active	Inactive	Inactive
1	1	0	Active	Active	Inactive
1	1	1	Active	Active	Active

Figure 2 illustrates the activity of the ICA, CCA, and DCA over a sample charge/discharge cycle of a battery pack, assuming the DS2438 is configured for the ICA to function and the CCA/DCA to function and shadow data to EEPROM. To simplify the illustration of the accumulators, they are treated as analog values, although they are digital counters in the DS2438. Note that when the battery becomes fully discharged, i.e., the ICA value reaches 0, the CCA and DCA register values are maintained.

CURRENT ACCUMULATOR ACTIVITY Figure 2



SENSE RESISTOR SELECTION

The selection of R_{SENS} involves a tradeoff. On the one hand, the impedance of R_{SENS} must be minimized to avoid excessive voltage drop during peak current demands. On the other hand, the impedance of R_{SENS} should be maximized to achieve the finest resolution for current measurement and accumulation. Table 9 below lists several example R_{SENS} values, the LSb of the current calculation ($1/(4096 * R_{SENS})$) and the LSb of the remaining capacity calculation ($1/(2048 * R_{SENS})$). The user should carefully consider voltage drop at maximum current and required current measurement/accumulation resolution when selecting R_{SENS}.

SENSE RESISTOR TRADEOFFS Table 9

SENSE RESISTOR VALUE (R_{SENS})	CURRENT lsb	REMAINING CAPACITY lsb	MAX REMAINING CAPACITY VALUE
25 mΩ	9.76 mA	19.53 mAHr	5000 mAhr
50 mΩ	4.88 mA	9.76 mAHr	2500 mAhr
100 mΩ	2.44 mA	4.88 mAHr	1250 mAhr
200 mΩ	1.22 mA	2.44 mAHr	625 mAhr

OPERATION - ELAPSED TIME METER

An internal oscillator is used as the timebase for the timekeeping functions. The elapsed time functions are double buffered, allowing the master to read elapsed time without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the 8th bit of the Recall Memory command.

The elapsed time meter (ETM) is a 4-byte binary counter with 1-second resolution. The ETM can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point, which is determined by the user. For example, 12:00 A.M., January 1, 1970 could be used as a reference point.

Two other time-related functions are available. The first is the Disconnect Timestamp, which is written to by the DS2438 whenever it senses that the DQ line has been low for approximately 2 seconds. This condition would signal that the battery pack has been removed from the system; the time when that occurs is written into the Disconnect Timestamp register, so that upon replacement into the system, the system can determine how long the device has been in storage, to facilitate self-discharge corrections to the remaining battery capacity. After the disconnect has been detected, the DS2438 reverts to a sleep mode, during which nothing is active except the real time clock. Some applications may prefer that the data converters and current accumulators continue operation following a pack disconnect. Thus, a version of the DS2438 (part number DS2438A) is offered for those applications. Other than not reverting to a low-power sleep mode following disconnect, there are no specification differences between the DS2438 and the DS2438A.

The other timestamp is the End-of-Charge timestamp, which is written to by the DS2438 whenever it senses that charging is finished (when current changes direction). This timestamp allows the user to calculate the amount of time the battery has been in a discharge or storage state, again to facilitate self-discharge calculations.

The format of the ETM, Disconnect, and End-of-Charge registers are as shown in Table 10. Refer to the "Memory Map" section for the address location of the time-related registers.

TIME REGISTER FORMAT Table 10

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB
MSb				(unit = 1s)			LSb	
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	
MSb				(unit = 1s)			LSb	
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	
MSb				(unit = 1s)			LSb	
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	MSB

64-BIT LASERED ROM

Each DS2438 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code (DS2438 code is 26h). The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 3.) The 64-bit ROM and ROM Function Control section allow the DS2438 to operate as a 1-Wire device and follow the 1-Wire protocol detailed in the section "1-Wire Bus System." The functions required to control sections of the DS2438 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM function protocol flow chart (Figure 5). The 1-Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. After a ROM function sequence has been successfully executed, the functions specific to the DS2438 are accessible and the bus master may then provide any one of the six memory and control function commands.

64-BIT LASERED ROM FORMAT Figure 3

8-BIT CRC CODE		48-BIT SERIAL NUMBER		8-BIT FAMILY CODE (26h)	
MSb	LSb	MSb	LSb	MSb	LSb

CRC Generation

The DS2438 has an 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS2438 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The DS2438 also generates an 8-bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of data bytes. In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8-bit CRC value stored in the 64-bit ROM portion of the DS2438 (for ROM reads) or the 8-bit CRC value computed within the DS2438 (which is read as a 9th byte when a scratchpad is read). The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS2438 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS2438 does not match the value generated by the bus master. Proper use of the CRC as outlined in the flowchart of Figure 6 can result in a communication channel with a very high level of integrity.

The 1-Wire CRC can be generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in Application Note 27 entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products."

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8^{th} bit of the family code has been entered, the serial number is entered. After the 48^{th} bit of the serial number has been entered, the shift register contains the CRC value.

1-WIRE CRC CODE Figure 4