Page 0 (00h)

The first page contains the most frequently accessed information of the DS2438, and most locations are volatile read-only bytes with the exception of the Status/Configuration Register (Byte 0) and the Threshold Register (Byte 7). The Status/Configuration Register is a nonvolatile read/write byte which defines which features of the DS2438 are enabled and how they will function. The register is formatted as follows:

X	ADB	NVB	TB	AD	EE	CA	IAD

MSb LSb

IAD = Current A/D Control Bit. "1" = the current A/D and the ICA are enabled, and current measurements will be taken at the rate of 36.41 Hz; "0" = the current A/D and the ICA have been disabled. The default value of this bit is a "1" (current A/D and ICA are enabled).

CA = Current Accumulator Configuration. "1" = CCA/DCA is enabled, and data will be stored and can be retrieved from page 7, bytes 4-7; "0" = CCA/DCA is disabled, and page 7 can be used for general EEPROM storage. The default value of this bit is a "1" (current CCA/DCA are enabled).

EE = Current Accumulator Shadow Selector bit. "1" = CCA/DCA counter data will be shadowed to EEPROM each time the respective register is incremented; "0"= CCA/DCA counter data will not be shadowed to EEPROM. The CCA/DCA could be lost as the battery pack becomes discharged. If the CA bit in the status/configuration register is set to "0", the EE bit will have no effect on the DS2438 functionality. The default value of this bit is a "1" (current CCA/DCA data shadowed to EEPROM).

AD = Voltage A/D Input Select Bit. "1" = the battery input (VDD) is selected as the input for the DS2438 voltage A/D converter; "0" = the general purpose A/D input (VAD) is selected as the voltage A/D input. For either setting, a Convert V command will initialize a voltage A/D conversion. The default value of this bit is a "1" (V_{DD} is the input to the A/D converter).

TB = Temperature Busy Flag. "1" = temperature conversion in progress; "0" = temperature conversion complete.

NVB = Nonvolatile Memory Busy Flag. "1" = Copy from Scratchpad to EEPROM in progress; "0" = Nonvolatile memory not busy. A copy to EEPROM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

ADB = A/D Converter Busy Flag. "1" = A/D conversion in progress on battery voltage; "0" = conversion complete, or no measurement being made. An A/D conversion takes approximately 10 ms.

X = Don't care

Bytes 1 and 2 of page 0 contain the last completed temperature conversion in the format described in the "Operation - Measuring Temperature" section. Bytes 3-4 contain the last completed voltage A/D conversion result and bytes 5-6 contain the instantaneous current data. Byte 7 contains the Threshold Register. Refer to the appropriate section for the data format of these locations.

NOTE:

The data in the scratchpad of the status and threshold register will determine the operation of the device.

Page 1 (01h)

The second page, Page 1, contains the ICA, elasped time meter, and current offset data. Both the ETM and ICA are volatile read/write locations so that they may be set, changed, or cleared by the host software. Bytes 0-3 contain the ETM data, formatted as described in the "Operation - Elapsed Time Meter" section. Byte 4 contains the 8-bit ICA. Bytes 5 and 6 contain the Offset Register data. Byte 7 is reserved and will read out as all "1"s.

Page 2 (02h)

The third page of memory (Page 2) contains the Disconnect (first 4 bytes) and End of Charge (remaining 4 bytes) timestamps. This page is volatile and read/write. Refer to the "Operation – Elapsed Time Meter" section for the formatting of these locations.

Pages 3-7 (03h - 07h)

The remainder of the memory in the DS2438 (Pages 3 through 7) is backed with EEPROM. This memory provides 40 bytes of user memory which may be used to carry any information the user wishes to store. Additionally, the CCA/DCA information is stored in bytes 4-7 of page 7 if the DS2438 is configured appropriately. If the CCA/DCA is used, page 7 should not be written to or current accumulator data will be overwritten. See "Operation-Current Accumulators" for details.

MEMORY MAP Figure 7

PAGE	BYTE	CONTENTS	R/W	NV
0	0	STATUS/ CONFIGURATION	R/W	YES
	1	TEMPERATURE LSB	R	NO
	2	TEMPERATURE MSB	R	NO
	3	VOLTAGE LSB	R	NO
	4	VOLTAGE MSB	R	NO
	5	CURRENT LSB	R	NO
	6	CURRENT MSB	R	NO
	7	THRESHOLD	R/W	YES
1	0	ETM BYTE 0	R/W	NO
	1	ETM BYTE 1	R/W	NO
	2	ETM BYTE 2	R/W	NO
	3	ETM BYTE 3	R/W	NO
	4	ICA	R/W	NO
	5	OFFSET LSB	R/W	YES
	6	OFFSET MSB	R/W	YES
	7	RESERVED	R/W	NO
2	0	DISCONNECT BYTE 0	R/W	NO
	1	DISCONNECT BYTE 1	R/W	NO
	2	DISCONNECT BYTE 2	R/W	NO
	3	DISCONNECT BYTE 3	R/W	NO
	4	END OF CHARGE BYTE 0	R/W	NO
	5	END OF CHARGE BYTE 1	R/W	NO
	6	END OF CHARGE BYTE 2	R/W	NO
	7	END OF CHARGE BYTE 3	R/W	NO
3	0	USER BYTE	R/W	YES
	1	USER BYTE	R/W	YES
	2	USER BYTE	R/W	YES
	3	USER BYTE	R/W	YES
	4	USER BYTE	R/W	YES
	5	USER BYTE	R/W	YES
	6	USER BYTE	R/W	YES
	7	USER BYTE	R/W	YES
4	0	USER BYTE	R/W	YES
	1	USER BYTE	R/W	YES
	2	USER BYTE	R/W	YES
	3	USER BYTE	R/W	YES
	4	USER BYTE	R/W	YES
	5	USER BYTE	R/W	YES
	6	USER BYTE	R/W	YES
	7	USER BYTE	R/W	YES
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
7	0	USER BYTE	R/W	YES
	1	USER BYTE	R/W	YES
	2	USER BYTE	R/W	YES
	3	USER BYTE	R/W	YES
	4	USER BYTE/ CCA LSB	R/W	YES
	5	USER BYTE/ CCA MSB	R/W	YES
	6	USER BYTE/ DCA LSB	R/W	YES
	7	USER BYTE/ DCA MSB	R/W	YES

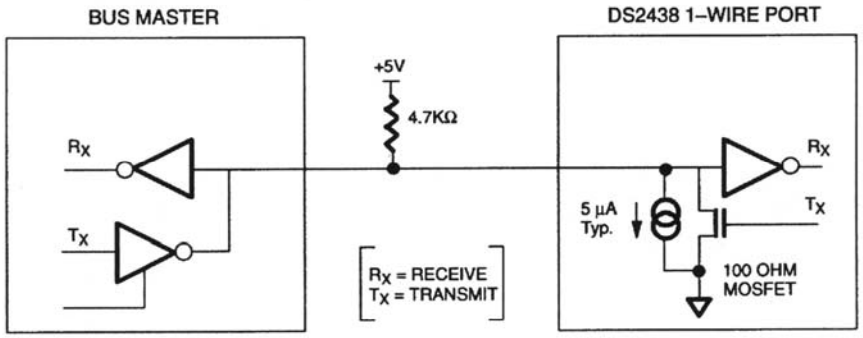
1-Wire BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. The DS2438 behaves as a slave. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS2438 (DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus requires a pull-up resistor of approximately 5 kΩ.

HARDWARE CONFIGURATION Figure 8



The idle state for the 1 wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If this does not occur and the bus is left low, all components on the bus will be reset. See Wire-1 Reset Pulse Timing (Figure 9).

TRANSACTION SEQUENCE

The protocol for accessing the DS2438 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2438 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8-bits long. A list of these commands follows (refer to flowchart in Figure 5):

Read ROM [33h]

This command allows the bus master to read the DS2438's 8-bit family code (26h), unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2438 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open-drain will produce a wired-AND result).

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2438 on a multidrop bus. Only the DS2438 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wired-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Example of a ROM Search

The ROM search process is the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-Wire bus. The ROM data of the four devices is as shown (LSb first):

ROM1 = 00110101...
ROM2 = 10101010...
ROM3 = 11110101...
ROM4 = 00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.

2. The bus master will then issue the search ROM command on the 1-Wire bus (F0h).

3. The bus master reads a bit from the 1-Wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 0 onto the 1-Wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-Wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line; therefore the bus master sees a 0. The bus master reads another bit. Since the Search ROM data command is being executed, all of the devices on the 1-Wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 1 onto the 1-wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-Wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the three-step routine have the following interpretations:

   00 - There are still devices attached which have conflicting bits in this position.
   01 - All devices still coupled have a 0 bit in this bit position.
   10 - All devices still coupled have a 1 bit in this bit position.
   11 - There are no devices attached to the 1-Wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-Wire bus.

5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0s as their second ROM data bit.

6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the 3rd bit of the ROM data of the attached devices.

8. The bus master writes a 0 bit. This deselects ROM1, leaving ROM4 as the only device still connected.

9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-Wire bus.

10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.

12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15. The bus master executes two read time slots and receives two 0s.

16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18. The bus master starts a new ROM search by repeating steps 13 through 15.

19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.

20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

Note that the bus master learns the unique ID number (ROM data pattern) of one 1-Wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

960 µs + (8 + 3 x 64) 61 µs = 13.16 ms

The bus master is therefore capable of identifying 75 different 1-Wire devices per second.

MEMORY COMMAND FUNCTIONS

The following command protocols are summarized in Table 11, and by the flowchart of Figure 6.

Write Scratchpad [4Ehxxh]

This command writes to the scratchpad page xxh of the DS2438. The entire 8-byte scratchpad space may be written, but all writing begins with the byte present at address 0 of the selected scratchpad. After issuing this command, the user must send the page number of the scratchpad to be written; then the user may begin writing data to the DS2438 scratchpad. Writing may be terminated at any point by issuing a reset. Valid page numbers for writing are 00h-07h.

Read Scratchpad [BEhxxh]

This command reads the contents of the scratchpad page xxh on the DS2438. After issuing this command, the user must send the page number of the scratchpad to be read, and then may begin reading the data, always beginning at address 0 of the selected scratchpad. The user may read through the end of the scratchpad space (byte 07h), with any reserved data bits reading all logic 1s, then read the CRC of the data, and after which the data read will be all logic 1s. If not all locations are to be read, the master may issue a reset to terminate reading at any time. Valid page numbers are 00h - 07h.

Copy Scratchpad [48hxxh]

This command copies the scratchpad page xxh into the EEPROM / SRAM memory page xxh of the DS2438. After issuing this command, the user must write a page number to direct which page of memory the scratchpad is to be copied. Valid page numbers are 00h - 07h. During the copy function, the NVB bit in the Status/Configuration register will be set to a "l". When the copy is complete, this bit will reset to "0". If the bus master issues read time slots following this command, the DS2438 will output "0" on the bus as long as it is busy copying the scratchpad to SRAM/EEPROM; it will return a "1" when the copy process is complete.

Recall Memory [B8hxxh]

This command recalls the stored values in EEPROM / SRAM page xxh to the scratchpad page xxh. This command must proceed a Read SPxx command in order to read any page of memory on the DS2438. Valid page numbers are 00h - 07h.

Convert T [44h]

This command begins a temperature conversion. No further data is required. The temperature conversion will be performed, setting the TB flag in the Status/Configuration register to a "1" during conversion. When the temperature conversion is done, the TB flag will clear to a "0". If the bus master issues read time slots following this command, the DS2438 will output "0" on the bus as long as it is busy making a temperature conversion; it will return a "1" when the temperature conversion is complete.

Convert V [B4h]

This command instructs the DS2438 to initiate a voltage analog-to-digital conversion cycle. This sets the ADB flag (see Status/Configuration register discussion in the Memory Map section). The voltage supply that is measured is defined by the AD bit of the Status/Configuration register. When the A/D conversion is done, the ADB flag is cleared and the current voltage value is placed in the VOLTAGE REGISTER of page 00h. While an A/D conversion is taking place, all other memory functions are still available for use. If the bus master issues read time slots following this command, the DS2438 will output "0" on the bus as long as it is busy making a voltage measurement; it will return a "1" when the conversion is complete.

DS2438 COMMAND SET Table 11

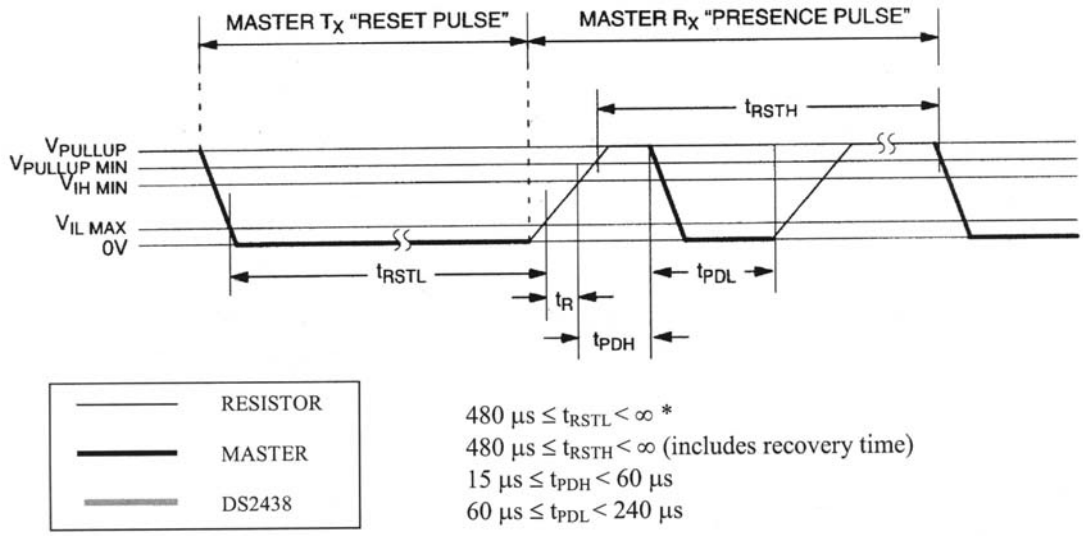
INSTRUCTION	DESCRIPTION	PROTOCOL	1-WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1-WIRE BUS DATA AFTER ISSUING PROTOCOL
MEMORY COMMANDS				
Read Scratchpad	Reads bytes from DS2438 Scratchpad page xxh	BEh <page 00h-07h>	Rx	<read up to nine bytes of data>
Write Scratchpad	Writes bytes to DS2438 Scratchpad page xxh	4Eh <page 00h-07h>	Tx	<write up to eight bytes of data>
Copy Scratchpad	Copies entire contents of Scratchpad page xxh to 8-byte EEPROM/ SRAM page xxh	48h<page 00h-07h>	Idle or Rx of NVB bit	{NVB bit in Status Register = 1 until copy complete (2-10 ms, typ)}
Recall Memory	Copies entire contents of EEPROM/SRAM page xxh to Scratchpad page xxh	B8h<page 00h-07h>	Idle	Idle
REGISTER COMMANDS				
Convert T	Initiates temperature conversion	44h	Idle or Rx of TB bit	{TB bit in Status Register = 1 until conversion complete}
Convert V	Initiates voltage A/D conversion	B4h	Idle or Rx of ADB bit	{ADB bit in Status Register = 1 until conversion complete}

SAMPLE COMMAND SEQUENCE Table 13

Example: Bus Master issues a temperature and voltage conversion, then reads the temperature, battery voltage, battery current, all on a single DS2438.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	44h	Issue Convert Temperature command, Read Slots
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	B4h	Issue Convert Voltage command, Read Slots
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	B8h00h	Issue Recall Memory page 00h command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Skip ROM
TX	BEh00h	Issue Read SP 00h command
RX	<9 data bytes>	Read scratchpad data and CRC. This page contains temperature, voltage, and current measurements.
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9



480 µs ≤ t_{RSTL} < ∞ *
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)
15 µs ≤ t_{PDH} < 60 µs
60 µs ≤ t_{PDL} < 240 µs

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high (inactive) logic level to a low logic level. There are two types of write time slots: Write 1 time slots and Write 0 time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2438 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write 1 occurs. If the line is low, a Write 0 occurs (See Figure 10).

For the host to generate a Write 1 time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot. For the host to generate a Write 0 time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

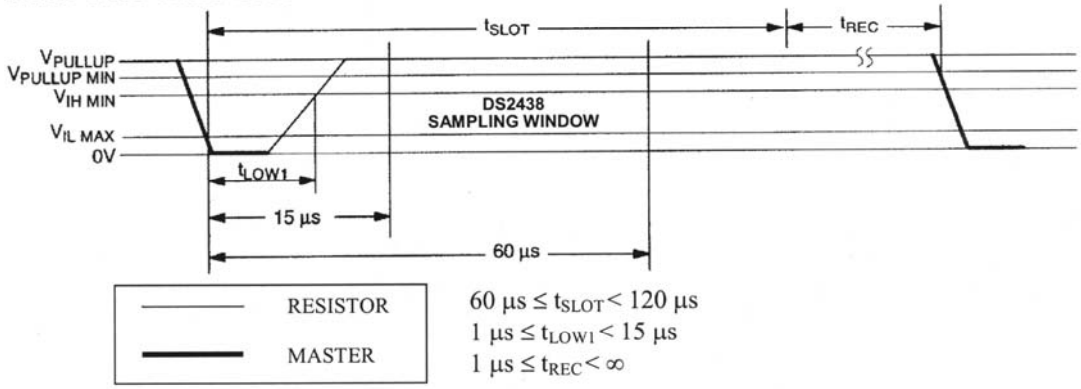
Read Time Slots

The host generates read time slots when data is to be read from the DS2438. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2438 is then valid within the next 14 µs maximum.

The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot. (see Figure 10). By the end of the read time slot, the I/O pin will pull back high via the external pull-up resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots.

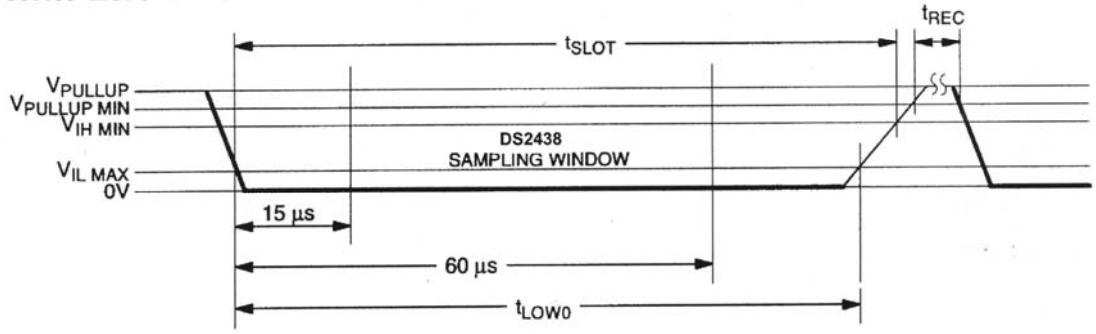
READ / WRITE TIMING DIAGRAM Figure 10

Write-One Time Slot



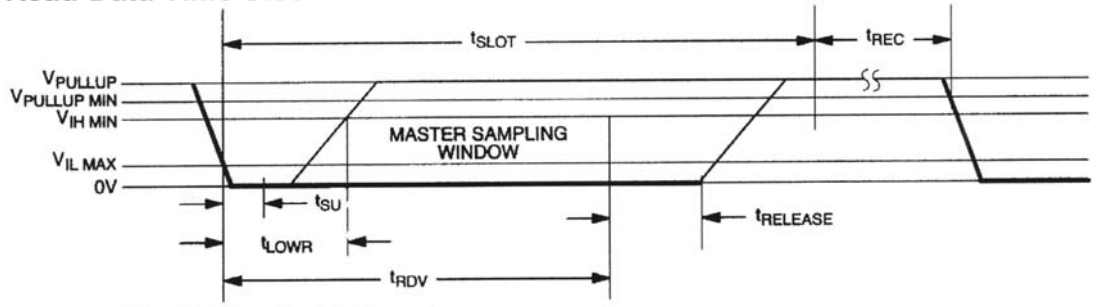
60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

Write-Zero Time Slot



60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs
1 µs ≤ t_{REC} < ∞

Read-Data Time Slot

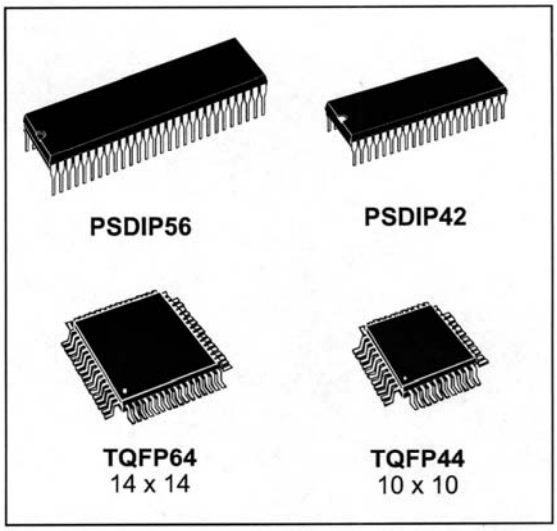


60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOWR} < 15 µs
0 ≤ $t_{RELEASE}$ < 45 µs
1 µs ≤ t_{REC} < ∞
t_{RDV} = 15 µs
t_{SU} < 1µs

ST72334J/N, ST72314J/N, ST72124J

8-BIT MCU WITH SINGLE VOLTAGE FLASH MEMORY, ADC, 16-BIT TIMERS, SPI, SCI INTERFACES

- **Memories**
  - 8K or 16K Program memory (ROM or single voltage FLASH) with read-out protection and in-situ programming (remote ISP)
  - 256 bytes EEPROM Data memory (with read-out protection option in ROM devices)
  - 384 or 512 bytes RAM
- **Clock, Reset and Supply Management**
  - Enhanced reset system
  - Enhanced low voltage supply supervisor with 3 programmable levels
  - Clock sources: crystal/ceramic resonator oscillators or RC oscillators, external clock, backup Clock Security System
  - 4 Power Saving Modes: Halt, Active-Halt, Wait and Slow
  - Beep and clock-out capabilities
- **Interrupt Management**
  - 10 interrupt vectors plus TRAP and RESET
  - 15 external interrupt lines (4 vectors)
- **44 or 32 I/O Ports**
  - 44 or 32 multifunctional bidirectional I/O lines:
  - 21 or 19 alternate function lines
  - 12 or 8 high sink outputs
- **4 Timers**
  - Configurable watchdog timer
  - Realtime base
  - Two 16-bit timers with: 2 input captures (only one on timer A), 2 output compares (only one on timer A), External clock input on timer A, PWM and Pulse generator modes
- **2 Communications Interfaces**
  - SPI synchronous serial interface
  - SCI asynchronous serial interface (LIN compatible)



- **1 Analog Peripheral**
  - 8-bit ADC with 8 input channels (6 only on ST72334Jx, not available on ST72124J2)
- **Instruction Set**
  - 8-bit data manipulation
  - 63 basic instructions
  - 17 main addressing modes
  - 8 x 8 unsigned multiply instruction
  - True bit manipulation
- **Development Tools**
  - Full hardware/software development package

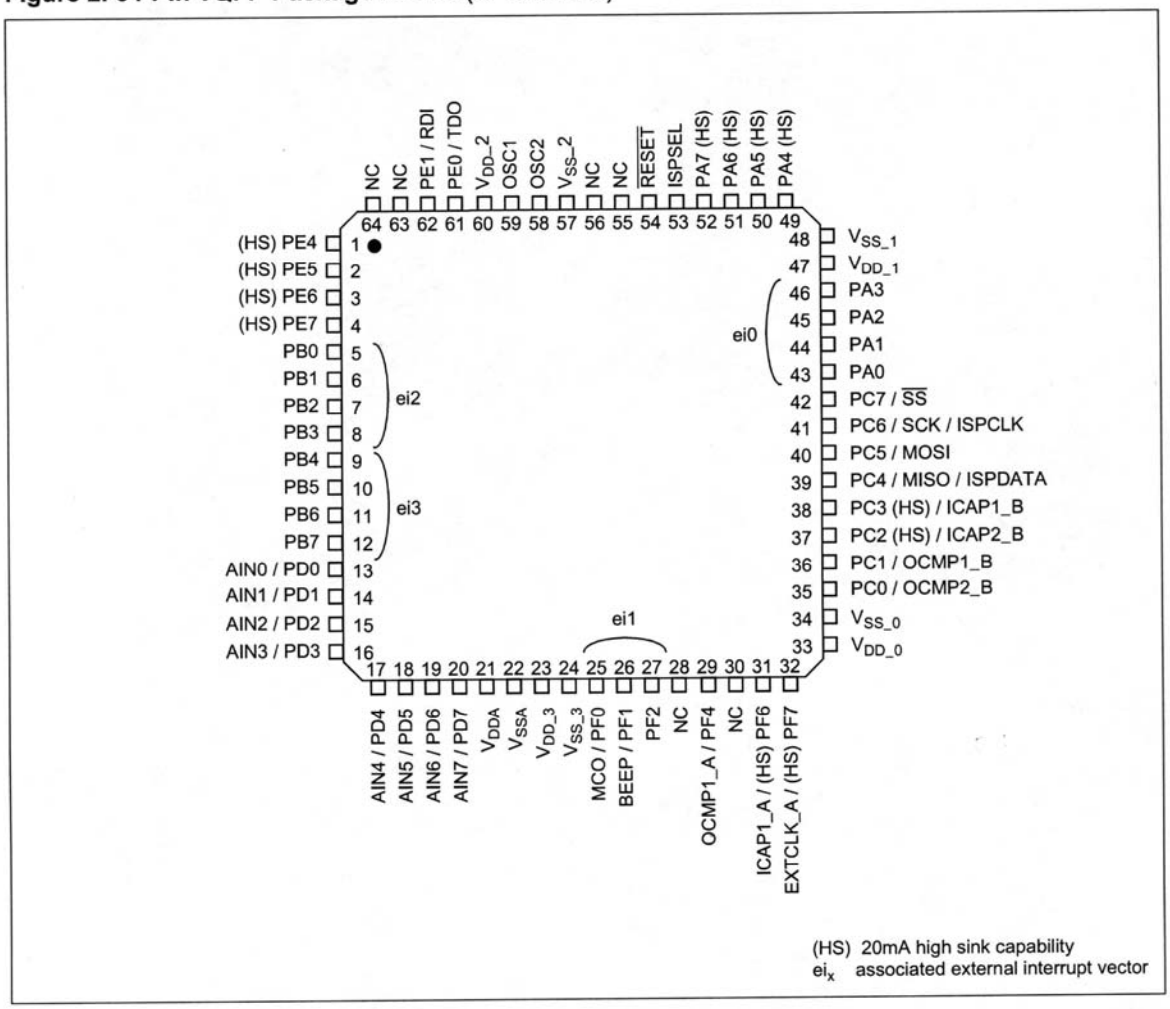
Device Summary

Features	ST72124J2	ST72314J2	ST72314J4	ST72314N2	ST72314N4	ST72334J2	ST72334J4	ST72334N2	ST72334N4
Program memory - bytes	8K	8K	16K	8K	16K	8K	16K	8K	16K
RAM (stack) - bytes	384 (256)	384 (256)	512 (256)	384 (256)	512 (256)	384 (256)	512 (256)	384 (256)	512 (256)
EEPROM - bytes	-	-	-	-	-	256	256	256	256
Peripherals	Watchdog, Two 16-bit Timers, SPI, SCI								
	-	ADC							
Operating Supply	3.2V to 5.5V								
CPU Frequency	Up to 8 MHz (with up to 16 MHz oscillator)								
Operating Temperature	-40°C to +85°C (-40°C to +105/125°C optional)								
Packages	TQFP44 / SDIP42			TQFP64 / SDIP56		TQFP44 / SDIP42		TQFP64 / SDIP56	

Rev. 2.4

3 PIN DESCRIPTION

Figure 2. 64-Pin TQFP Package Pinout (N versions)



5 FLASH PROGRAM MEMORY

5.1 INTRODUCTION

FLASH devices have a single voltage non-volatile FLASH memory that may be programmed in-situ (or plugged in a programming tool) on a byte-by-byte basis.

5.2 MAIN FEATURES

- Remote In-Situ Programming (ISP) mode
- Up to 16 bytes programmed in the same cycle
- MTP memory (Multiple Time Programmable)
- Read-out memory protection against piracy

5.3 STRUCTURAL ORGANISATION

The FLASH program memory is organised in a single 8-bit wide memory block which can be used for storing both code and data constants.

The FLASH program memory is mapped in the upper part of the ST7 addressing space and includes the reset and interrupt user vector area .

5.4 IN-SITU PROGRAMMING (ISP) MODE

The FLASH program memory can be programmed using Remote ISP mode. This ISP mode allows the contents of the ST7 program memory to be updated using a standard ST7 programming tools after the device is mounted on the application board. This feature can be implemented with a minimum number of added components and board area impact.

An example Remote ISP hardware interface to the standard ST7 programming tool is described below. For more details on ISP programming, refer to the ST7 Programming Specification.

Remote ISP Overview

The Remote ISP mode is initiated by a specific sequence on the dedicated ISPSEL pin.

The Remote ISP is performed in three steps:

- Selection of the RAM execution mode
- Download of Remote ISP code in RAM
- Execution of Remote ISP code in RAM to program the user program into the FLASH

Remote ISP hardware configuration

In Remote ISP mode, the ST7 has to be supplied with power (V_{DD} and V_{SS}) and a clock signal (oscillator and application crystal circuit for example).

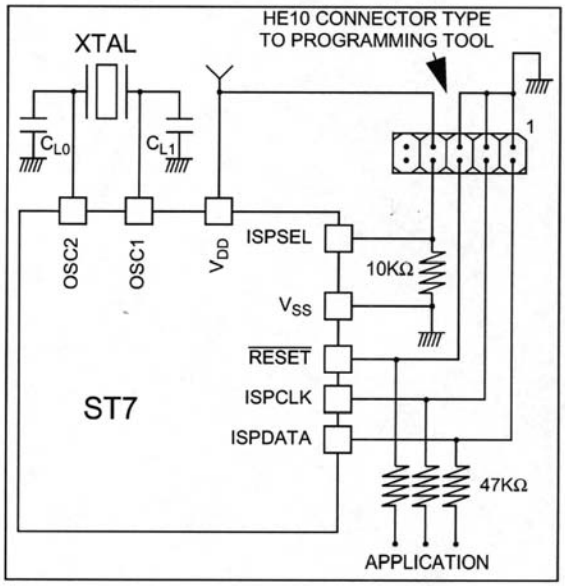
This mode needs five signals (plus the V_{DD} signal if necessary) to be connected to the programming tool. This signals are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device ground power supply
- ISPCLK: ISP output serial clock pin
- ISPDATA: ISP input serial data pin
- ISPSEL: Remote ISP mode selection. This pin must be connected to V_{SS} on the application board through a pull-down resistor.

If any of these pins are used for other purposes on the application, a serial resistor has to be implemented to avoid a conflict if the other device forces the signal level.

Figure 6 shows a typical hardware interface to a standard ST7 programming tool. For more details on the pin locations, refer to the device pinout description.

Figure 6. Typical Remote ISP Interface



5.5 MEMORY READ-OUT PROTECTION

The read-out protection is enabled through an option bit.

For FLASH devices, when this option is selected, the program and data stored in the FLASH memory are protected against read-out piracy (including a re-write protection). When this protection option is removed the entire FLASH program memory is first automatically erased. However, the E^2PROM data memory (when available) can be protected only with ROM devices.

14.4 SERIAL PERIPHERAL INTERFACE (SPI)

14.4.1 Introduction

The Serial Peripheral Interface (SPI) allows full-duplex, synchronous, serial communication with external devices. An SPI system may consist of a master and one or more slaves or a system in which devices may be either masters or slaves.

The SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Refer to the Pin Description chapter for the device-specific pin-out.

14.4.2 Main Features

- Full duplex, three-wire synchronous transfers
- Master or slave operation
- Four master mode frequencies
- Maximum slave mode frequency = $f_{CPU}/4$.
- Four programmable master bit rates
- Programmable clock polarity and phase
- End of transfer interrupt flag
- Write collision flag protection
- Master mode fault protection capability.

14.4.3 General description

The SPI is connected to external devices through 4 alternate pins:

- MISO: Master In Slave Out pin
- MOSI: Master Out Slave In pin
- SCK: Serial Clock pin
- $\overline{SS}$: Slave select pin

A basic example of interconnections between a single master and a single slave is illustrated on Figure 42.

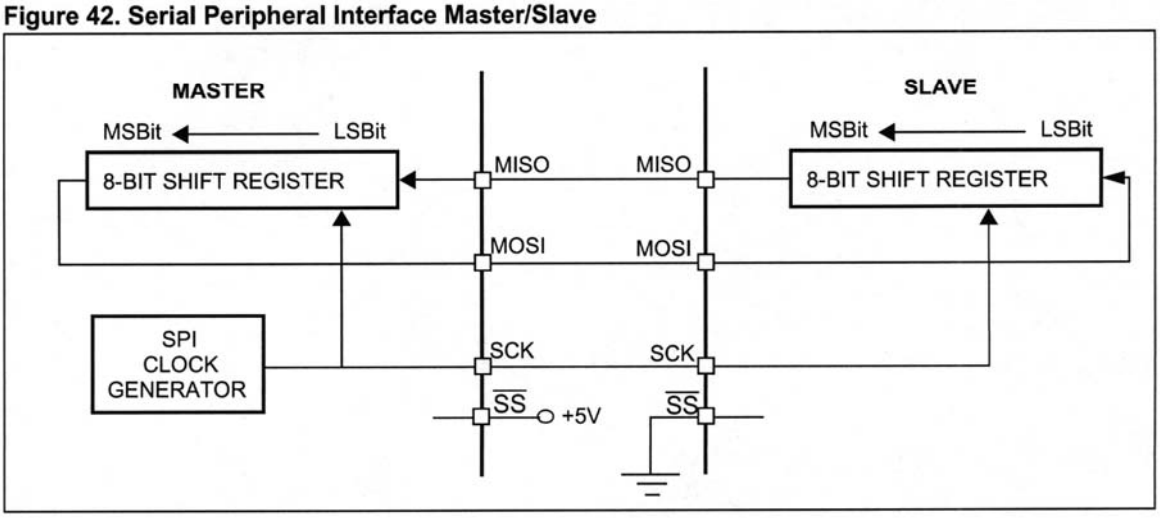
The MOSI pins are connected together as are MISO pins. In this way data is transferred serially between master and slave (most significant bit first).

When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full bits. A status flag is used to indicate that the I/O operation is complete.

Four possible data/clock timing relationships may be chosen (see Figure 45) but master and slave must be programmed with the same timing mode.

Figure 42. Serial Peripheral Interface Master/Slave



14.5 SERIAL COMMUNICATIONS INTERFACE (SCI)

14.5.1 Introduction

The Serial Communications Interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous

serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

14.5.2 Main Features

- Full duplex, asynchronous communications
- NRZ standard format (Mark/Space)
- Dual baud rate generator systems
- Independently programmable transmit and receive baud rates up to 250K baud using conventional baud rate generator and up to 500K baud using the extended baud rate generator.
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- Two receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- LIN compatible (if MCU clock frequency tolerance ≤2%)
- Separate enable bits for Transmitter and Receiver
- Three error detection flags:
  - Overrun error
  - Noise error
  - Frame error
- Five interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error detected

14.5.3 General Description

The interface is externally connected to another device by two pins (see Figure 49):

- TDO: Transmit Data Output. When the transmitter is disabled, the output pin returns to its I/O port configuration. When the transmitter is enabled and nothing is to be transmitted, the TDO pin is at high level.
- RDI: Receive Data Input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

Through this pins, serial data is transmitted and received as frames comprising:

- An Idle Line prior to transmission or reception
- A start bit
- A data word (8 or 9 bits) least significant bit first
- A Stop bit indicating that the frame is complete.

This interface uses two types of baud rate generator:

- A conventional type for commonly-used baud rates,
- An extended type with a prescaler offering a very wide range of baud rates even with non-standard oscillator frequencies.

14.5.4 LIN Protocol support

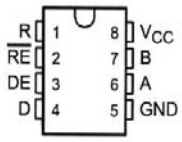
For LIN applications where resynchronization is not required (application clock tolerance less than or equal to 2%) the LIN protocol can be efficiently implemented with this standard SCI.

SN65176B, SN75176B
DIFFERENTIAL BUS TRANSCEIVERS

SLLS101B – JULY 1985 – REVISED JUNE 1999

- Bidirectional Transceivers
- Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operate From Single 5-V Supply

D OR P PACKAGE
(TOP VIEW)



description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN65176B is characterized for operation from −40°C to 105°C and the SN75176B is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Unitrode Products
from Texas Instruments

application INFO available

UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

Current Mode PWM Controller

FEATURES

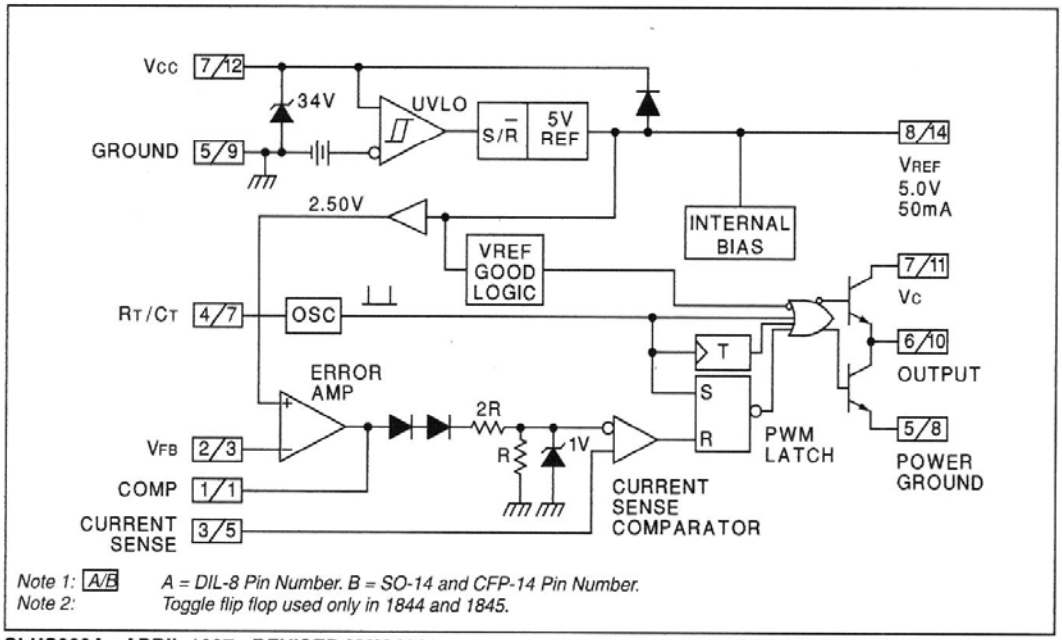
- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low RO Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 and CFP-14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

SLUS223A - APRIL 1997 - REVISED MAY 2002