National Semiconductor

July 1999

LMF100
High Performance Dual Switched Capacitor Filter

General Description

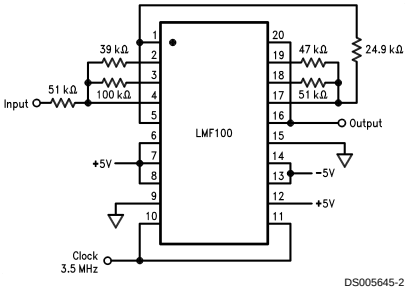
The LMF100 consists of two independent general purpose high performance switched capacitor filters. With an external clock and 2 to 4 resistors, various second-order and first-order filtering functions can be realized by each filter block. Each block has 3 outputs. One output can be configured to perform either an allpass, highpass, or notch function. The other two outputs perform bandpass and lowpass functions. The center frequency of each filter stage is tuned by using an external clock or a combination of a clock and resistor ratio. Up to a 4th-order biquadratic function can be realized with a single LMF100. Higher order filters are implemented by simply cascading additional packages, and all the classical filters (such as Butterworth, Bessel, Elliptic, and Chebyshev) can be realized.

The LMF100 is fabricated on National Semiconductor's high performance analog silicon gate CMOS process, LMCMOS™. This allows for the production of a very low offset, high frequency filter building block. The LMF100 is pin-compatible with the industry standard MF10, but provides greatly improved performance.

Features

- Wide 4V to 15V power supply range
- Operation up to 100 kHz
- Low offset voltage: typically
  (50:1 or 100:1 mode): Vos1 = ±5 mV
  Vos2 = ±15 mV
  Vos3 = ±15 mV
- Low crosstalk −60 dB
- Clock to center frequency ratio accuracy ±0.2% typical
- f_0 x Q range up to 1.8 MHz
- Pin-compatible with MF10

4th Order 100 kHz Butterworth Lowpass Filter



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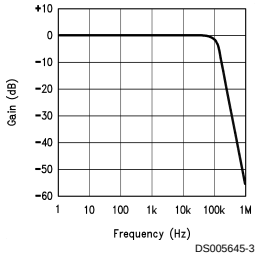

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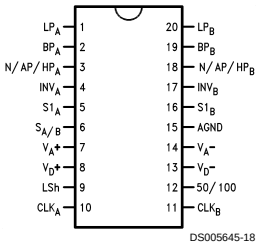
Connection Diagram

Surface Mount and Dual-In-Line Package



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Top View
Order Number
LMF100CCN or LMF100CIWM
See NS Package Number N20A or M20B

LMCMOS™ is a trademark of National Semiconductor Corporation.

VANTIS
AN AMD COMPANY

MACH® 4 Family

High Performance EE CMOS Programmable Logic With Maximum Ease Of Use

DISTINCTIVE CHARACTERISTICS

- **High-performance, EE CMOS CPLD family**
- **SpeedLocking™ for guaranteed fixed timing (-7/10/12/15 ns tPD)**
- **High density**
  - 1250-10,000 PLD Gates
  - 44-208 Pins
  - 32-384 Registers
- **32-256 macrocells**
  - D/T,J-K,S-R Registers and latches
  - Synchronous or asynchronous mode
  - Programmable polarity
  - Reset/preset swapping
- **Central, input, and output switch matrices**
  - 100% Routability
- **Input and output switch matrices for 100% pin-out retention**
- **JTAG in-system programmable**
- **Up to 20 product terms per macrocell, with XOR**
- **Registered/latched inputs**
- **Synchronous and asynchronous modes for each macrocell**
  - Clock generator in each PAL® block for programmable clocks, edges in either mode
  - Individual clock, initialization product terms in asynchronous mode
- **Extensive software development support**
- **Third-party hardware programming support**

PRODUCT SELECTOR GUIDE

Device	Package	Macrocells	I/Os	Dedicated Inputs	Output Enables	Flip-Flops	Commercial		Industrial	t_{SS} (ns)	t_{CO} (ns)	I_{CC} Static (mA)
							t_{PD} (ns)	f_{CNT} (MHz)	t_{PD} (ns)			
M4(LV)-32	44 PLCC 44 TQFP	32	32	2	32	32	7.5	133	10	5.5	5.5	35
M4(LV)-64	44 PLCC 44 TQFP	64	32	2	32	96	7.5	133	10	5.5	5.5	55
M4(LV)-96	100 TQFP	96	48	8	48	144	7.5	133	10	5.5	5.5	60
M4-96	144 PQFP	96	96	6	96	96	15	66.6	NA	NA	NA	188
M4(LV)-128	100 PQFP 100 TQFP	128	64	6	64	192	7.5	133	10	5.5	5.5	70
M4(LV)-128N	84 PLCC	128	64	6	64	192	7.5	133	10	5.5	5.5	70
M4(LV)-192	144 TQFP	192	96	16	96	288	10	100	12	6	6.5	85
M4(LV)-256	208 PQFP	256	128	14	128	384	10	100	12	6	6.5	100

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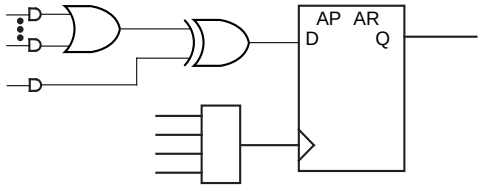
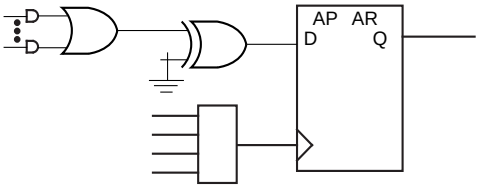
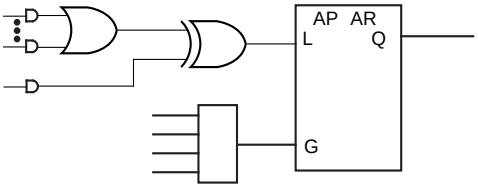
The flip-flop can be configured as a D-type, T-type, J-K, or S-R register or latch. The primary flip-flop configurations are shown in Figure 8, although others are possible. Flip-flop functionality is defined in Table 4. Note that a J-K latch is inadvisable, as it will cause oscillation if both J and K inputs are HIGH.



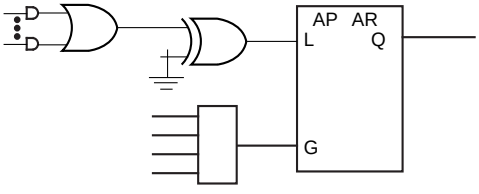
a. D-type with XOR



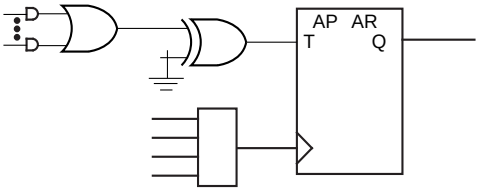
b. D-type with programmable D polarity



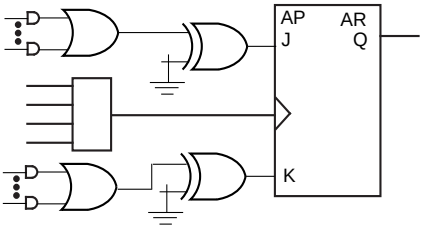
c. Latch with XOR



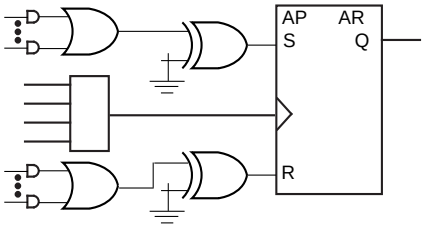
d. Latch with programmable polarity



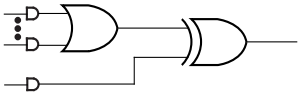
e. T-type with programmable T polarity



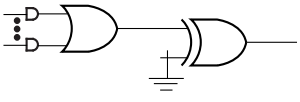
f. J-K with programmable J and K polarity



g. S-R with programmable S and R polarity



h. Combinatorial with XOR



i. Combinatorial with programmable polarity

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Figure 8. Primary Macrocell Configurations

Table 4. Register/Latch Operation

Configuration	Input(s)	CLK/LE*	Q+
D-type Register	D=X	0,1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ ↓	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
J-K Register	J=K=X	0,1, ↓ (↑)	Q
	J=0, K=0	↑ (↓)	Q
	J=0, K=1	↑ (↓)	0
	J=1, K=0	↑ (↓)	1
	J=1, K=1	↑ (↓)	$\overline{Q}$
S-R Register	S=R=X	0,1, O (↓)	Q
	S=0, R=0	↑ (↓)	Q
	S=0, R=1	↑ (↓)	0
	S=1, R=0	↑ (↓)	1
	S=1, R=1	↑ (↓)	Undefined
D-type Latch	D=X	1(0)	Q
	D=0	0(1)	0
	D=1	0(1)	1

**Polarity of CLK/LE can be programmed.*

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 9), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 14)

Supply Voltage ($V^+ - V^-$)	16V
Voltage at Any Pin	$V^+ + 0.3V$
	$V^- - 0.3V$
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	150˚C
ESD Susceptability (Note 11)	2000V
Soldering Information	
N Package: 10 sec.	260˚C
J Package: 10 sec.	300˚C
SO Package:	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF100CCN	$0˚C \le T_A \le +70˚C$
LMF100CIWM	$-40˚C \le T_A \le +85˚C$
Supply Voltage	$4V \le V^+ - V^- \le 15V$

Electrical Characteristics

The following specifications apply for Mode 1, Q = 10 ($R_1 = R_3 = 100k$, $R_2 = 10k$), $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25˚C$.

Symbol	Parameter		Conditions		LMF100CCN			LMF100CIWM			Units
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
I_s	Maximum Supply Current		f_{CLK} = 250 kHz No Input Signal		9	13	**13**	9	**13**		mA
f_0	Center Frequency	MIN			0.1			0.1			Hz
	Range	MAX			100			100			kHz
f_{CLK}	Clock Frequency	MIN			5.0			5.0			Hz
	Range	MAX			3.5			3.5			MHz
f_{CLK}/f_0	Clock to Center Frequency Ratio Deviation		V_{Pin12} = 5V or 0V f_{CLK} = 1 MHz		±0.2	±0.8	**±0.8**	±0.2	**±0.8**		%
$\frac{\Delta Q}{Q}$	Q Error (MAX) (Note 4)		Q = 10, Mode 1 V_{Pin12} = 5V or 0V f_{CLK} = 1 MHz		±0.5	±5	**±6**	±0.5	**±6**		%
H_{OBP}	Bandpass Gain at f_0		f_{CLK} = 1 MHz		0	±0.4	**±0.4**	0	±**0.4**		dB
H_{OLP}	DC Lowpass Gain		$R_1 = R_2$ = 10k f_{CLK} = 250 kHz		0	±0.2	**±0.2**	0	**±0.2**		dB
V_{OS1}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz		±5.0	±15	**±15**	±5.0	**±15**		mV
V_{OS2}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz	$S_{A/B} = V^+$	±30	±80	**±80**	±30	±**80**		mV
				$S_{A/B} = V^-$	±15	±70	**±70**	±15	±**70**		mV
V_{OS3}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz		±15	±40	±**60**	±15	±**60**		mV
	Crosstalk (Note 6)		A Side to B Side or B Side to A Side		−60			−60			dB
	Output Noise (Note 12)		f_{CLK} = 250 kHz	N	40			40			µV
			20 kHz Bandwidth	BP	320			320			
			100:1 Mode	LP	300			300			
	Clock Feedthrough (Note 13)		f_{CLK} = 250 kHz 100:1 Mode		6			6			mV
V_{OUT}	Minimum Output Voltage Swing		R_L = 5k (All Outputs)		+4.0 −4.7	±3.8	**±3.7**	+4.0 −4.7	**±3.7**		V
			R_L = 3.5k (All Outputs)		+3.9 −4.6			+3.9 −4.6			V
GBW	Op Amp Gain BW Product				5			5			MHz
SR	Op Amp Slew Rate				20			20			V/µs
I_{sc}	Maximum Output Short	Source	(All Outputs)		12			12			mA
	Circuit Current (Note 7)	Sink			45			45			mA

Electrical Characteristics (Continued)

The following specifications apply for Mode 1, Q = 10 (R_1 = R_3 = 100k, R_2 = 10k), V^+ = +5V and V^- = −5V unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C.

Symbol	Parameter	Conditions	LMF100CCN			LMF100CIWM			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
I_{IN}	Input Current on Pins: 4, 5, 6, 9, 10, 11, 12, 16, 17			10			**10**		µA

Electrical Characteristics

The following specifications apply for Mode 1, Q = 10 (R_1 = R_3 = 100k, R_2 = 10k), V^+ = +2.50V and V^- = −2.50V unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25˚C.

Symbol	Parameter		Conditions		LMF100CCN			LMF100CIWM			Units
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
I_s	Maximum Supply Current		f_{CLK} = 250 kHz No Input Signal		8	12	**12**	8	**12**		mA
f_0	Center Frequency	MIN			0.1			0.1			Hz
	Range	MAX			50			50			kHz
f_{CLK}	Clock Frequency	MIN			5.0			5.0			Hz
	Range	MAX			1.5			1.5			MHz
f_{CLK}/f_0	Clock to Center Frequency Ratio Deviation		V_{Pin12} = 2.5V or 0V f_{CLK} = 1 MHz		±0.2	±1	**±1**	±0.2	**±1**		%
$\frac{\Delta Q}{Q}$	Q Error (MAX) (Note 4)		Q = 10, Mode 1 V_{Pin12} = 5V or 0V f_{CLK} = 1 MHz		±0.5	±5	**±8**	±0.5	**±8**		%
H_{OBP}	Bandpass Gain at f_0		f_{CLK} = 1 MHz		0	±0.4	**±0.5**	0	**±0.5**		dB
H_{OLP}	DC Lowpass Gain		R_1 = R_2 = 10k f_{CLK} = 250 kHz		0	±0.2	**±0.2**	0	**±0.2**		dB
V_{OS1}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz		±5.0	±15	**±15**	±5.0	**±15**		mV
V_{OS2}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz	$S_{A/B}$ = V^+	±20	±60	**±60**	±20	**±60**		mV
				$S_{A/B}$ = V^-	±10	±50	**±60**	±10	**±60**		mV
V_{OS3}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz		±10	±25	**±30**	±10	**±30**		mV
	Crosstalk (Note 6)		A Side to B Side or B Side to A Side		−65			−65			dB
	Output Noise (Note 12)		f_{CLK} = 250 kHz	N	25			25			µV
			20 kHz Bandwidth	BP	250			250			
			100:1 Mode	LP	220			220			
	Clock Feedthrough (Note 13)		f_{CLK} = 250 kHz 100:1 Mode		2			2			mV
V_{OUT}	Minimum Output Voltage Swing		R_L = 5k (All Outputs)		+1.6 −2.2	±1.5	**±1.4**	+1.6 −2.2	**±1.4**		V
			R_L = 3.5k (All outputs)		+1.5 −2.1			+1.5 −2.1			V
GBW	Op Amp Gain BW Product				5			5			MHz
SR	Op Amp Slew Rate				18			18			V/µs
I_{sc}	Maximum Output Short Circuit Current (Note 7)	Source	(All Outputs)		10			10			mA
		Sink			20			20			mA

Logic Input Characteristics

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25^\circ C$.

Parameter		Conditions	LMF100CCN			LMF100CIWM			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CMOS Clock Input Voltage	MIN Logical "1"	$V^+ = +5V$, $V^- = -5V$,		+3.0	**+3.0**		**+3.0**		V
	MAX Logical "0"	$V_{LSh} = 0V$		−3.0	**−3.0**		**−3.0**		V
	MIN Logical "1"	$V^+ = +10V$, $V^- = 0V$,		+8.0	**+8.0**		**+8.0**		V
	MAX Logical "0"	$V_{LSh} = +5V$		+2.0	**+2.0**		**+2.0**		V
TTL Clock Input Voltage	MIN Logical "1"	$V^+ = +5V$, $V^- = -5V$,		+2.0	**+2.0**		**+2.0**		V
	MAX Logical "0"	$V_{LSh} = 0V$		+0.8	**+0.8**		**+0.8**		V
	MIN Logical "1"	$V^+ = +10V$, $V^- = 0V$,		+2.0	**+2.0**		**+2.0**		V
	MAX Logical "0"	$V_{LSh} = 0V$		+0.8	**+0.8**		**+0.8**		V
CMOS Clock Input Voltage	MIN Logical "1"	$V^+ = +2.5V$, $V^- = -2.5V$,		+1.5	**+1.5**		**+1.5**		V
	MAX Logical "0"	$V_{LSh} = 0V$		−1.5	**−1.5**		**−1.5**		V
	MIN Logical "1"	$V^+ = +5V$, $V^- = 0V$,		+4.0	**+4.0**		**+4.0**		V
	MAX Logical "0"	$V_{LSh} = +2.5V$		+1.0	**+1.0**		**+1.0**		V
TTL Clock Input Voltage	MIN Logical "1"	$V^+ = +5V$, $V^- = 0V$,		+2.0	**+2.0**		**+2.0**		V
	MAX Logical "0"	$V_{LSh} = 0V$, $V_D{}^+ = 0V$		+0.8	**+0.8**		**+0.8**		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125^\circ C$, and the typical junction-to-ambient thermal resistance of the LMF100CIN when board mounted is $55^\circ C/W$. For the LMF100CIWM this number is $66^\circ C/W$.

Note 4: The accuracy of the Q value is a function of the center frequency (f_0). This is illustrated in the curves under the heading "Typical Peformance Characteristics".

Note 5: V_{os1}, V_{os2}, and V_{os3} refer to the internal offsets as discussed in the Applications Information section 3.4.

Note 6: Crosstalk between the internal filter sections is measured by applying a 1 V_{RMS} 10 kHz signal to one bandpass filter section input and grounding the input of the other bandpass filter section. The crosstalk is the ratio between the output of the grounded filter section and the 1 V_{RMS} input signal of the other section.

Note 7: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Note 8: Typicals are at $25^\circ C$ and represent most likely parametric norm.

Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Design limits are guaranteed to National's AOQL (Average Outgoing Quality Level) but are not 100% tested.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

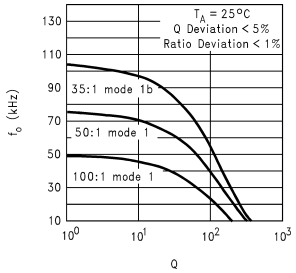
Note 12: In 50:1 mode the output noise is 3 dB higher.

Note 13: In 50:1 mode the clock feedthrough is 6 dB higher.

Note 14: A military RETS specification is available upon request.

Typical Performance Characteristics (Continued)

Maximum f_0 vs Q at V_s = ±7.5V



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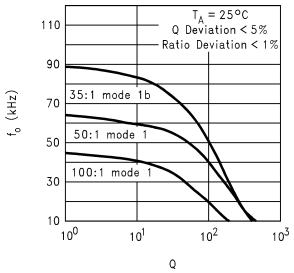
Maximum f_0 vs Q at V_s = ±5.0V



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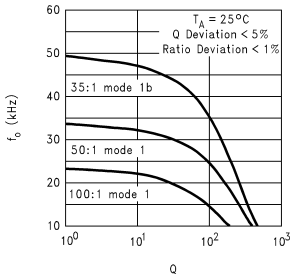
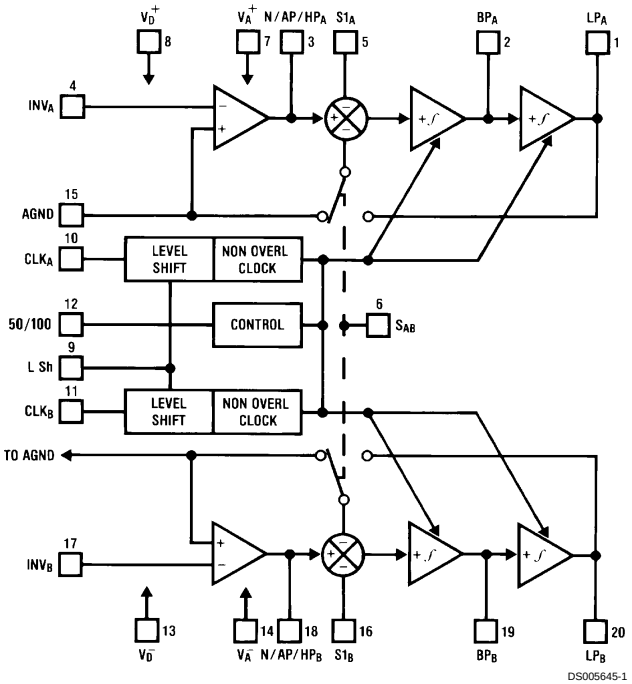
Maximum f_0 vs Q at V_s = ±2.5V



DS005645-63

LMF100 System Block Diagram



DS005645-1

Pin Descriptions

LP(1,20), BP(2,19), N/AP/HP(3,18)	The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically swing to within 1V of each supply when driving a 5 kΩ load. For optimum performance, capacitive loading on these outputs should be minimized. For signal frequencies above 15 kHz the capacitance loading should be kept below 30 pF.
INV(4,17)	The inverting input of the summing opamp of each filter. These are high impedance inputs. The non-inverting input is internally tied to AGND so the opamp can be used only as an inverting amplifier.
S1(5,16)	S1 is a signal input pin used in modes 1b, 4, and 5. The input impedance is $1/f_{CLK}$ x 1 pF. The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).
$S_{A/B}$(6)	This pin activates a switch that connects one of the inputs of each filter's second summer either to AGND ($S_{A/B}$ tied to V^-) or to the lowpass (LP) output ($S_{A/B}$ tied to V^+). This offers the flexibility needed for configuring the filter in its various modes of operation.
V_A^+(7) (Note 15)	This is both the analog and digital positive supply.
V_D^+(8) (Note 15)	This pin needs to be tied to V^+ except when the device is to operate on a single 5V supply and a TTL level clock is applied. For 5V, TTL operation, V_D^+ should be tied to ground (0V).
V_A^-(14), V_D^-(13)	Analog and digital negative supplies. $V_A^-$and V_D^- should be derived from the same source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can also be tied together externally and bypassed with a single capacitor.
LSh(9)	Level shift pin. This is used to accommodate various clock levels with dual or single supply operation. With dual ±5V supplies and CMOS (±5V) or TTL (0V–5V) clock levels, LSh should be tied to system ground. For 0V–10V single supply operation the AGND pin should be biased at +5V and the LSh pin should be tied to the system ground for TTL clock levels. LSh should be biased at +5V for ±5V CMOS clock levels. The LSh pin is tied to system ground for ±2.5V operation. For single 5V operation the LSh and V_D+ pins are tied to system ground for TTL clock levels.
CLK(10,11)	Clock inputs for the two switched capacitor filter sections. Unipolar or bipolar clock levels may be applied to the CLK inputs according to the programming voltage applied to the LSh pin. The duty cycle of the clock should be close to 50%, especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal opamps to settle, which yields optimum filter performance.
50/100(12) (Note 15)	By tying this pin to V^+ a 50:1 clock to filter center frequency ratio is obtained. Tying this pin at mid-supply (i.e., system ground with dual supplies) or to V^- allows the filter to operate at a 100:1 clock to center frequency ratio.
AGND(15)	This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

Note 15: This device is pin-for-pin compatible with the MF10 except for the following changes:

1. Unlike the MF10, the LMF100 has a single positive supply pin (V_A+).

2. On the LMF100 V_D^+ is a control pin and is not the digital positive supply as on the MF10.

3. Unlike the MF10, the LMF100 does not support the current limiting mode. When the 50/100 pin is tied to V^- the LMF100 will remain in the 100:1 mode.

1.0 Definitions of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 10 or 11.

f_0: center frequency of the second order function complex pole pair. f_0 is measured at the bandpass outputs of the LMF100, and is the frequency of maximum bandpass gain. (*Figure 1*).

f_{notch}: the frequency of minimum (ideally zero) gain at the notch outputs.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_0 and if Q_z is high, it can be observed as the frequency of a notch at the allpass output. (*Figure 13*).

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass outputs of the LMF100 and is equal to f_0 divided by the −3 dB bandwidth of the 2nd order bandpass filter (*Figure 1*). The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

Q_z: the quality factor of the second order complex zero pair, if any. Q_Z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q_z} + \omega_o{}^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o{}^2}$$

where $Q_Z = Q$ for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at $f = f_0$.

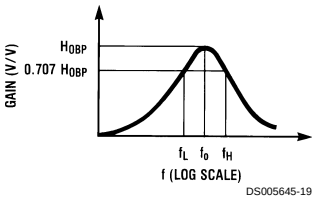
H_{OLP}: the gain (in V/V) of the lowpass output as $f \rightarrow 0$ Hz (*Figure 2*).

H_{OHP}: the gain (in V/V) of the highpass output as $f \rightarrow f_{CLK}/2$ (*Figure 3*).

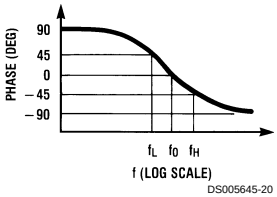
H_{ON}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz and as $f \rightarrow f_{CLK}/2$, when the notch filter has equal gain above and below the center frequency (*Figure 4*). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (*Figure 10* and *Figure 12*), the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz.

H_{ON2}: the gain (in V/V) of the notch output as $f \rightarrow f_{CLK}/2$.



(a)



(b)

$$H_{BP}(s) = \frac{\frac{\omega_O}{Q}s}{s^2 + \frac{s\omega_o}{Q} + \omega_o{}^2}$$

$$Q = \frac{f_0}{f_H - f_L};\ f_0 = \sqrt{f_L f_H}$$

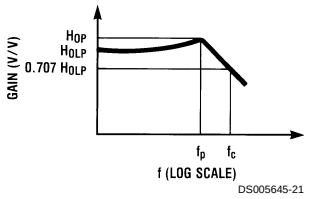
$$f_L = f_0\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_0\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

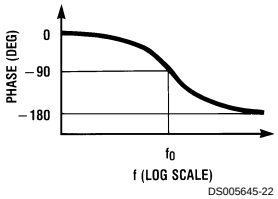
$$\omega_o = 2\pi f_0$$

FIGURE 1. 2nd-Order Bandpass Response

1.0 Definitions of Terms (Continued)



(a)



(b)

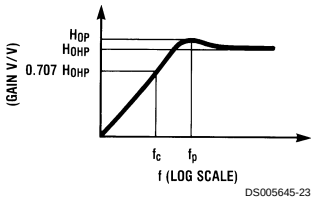
$$H_{LP}(s) = \frac{H_{OLP}\omega_O^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$f_c = f_0 \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

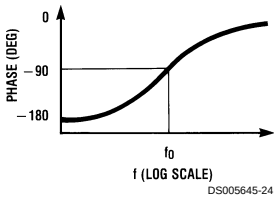
$$f_p = f_0 \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2. 2nd-Order Low-Pass Response



(a)



(b)

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

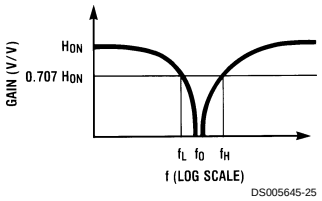
$$f_c = f_0 \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_p = f_0 \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

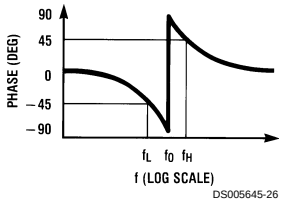
$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 3. 2nd-Order High-Pass Response

1.0 Definitions of Terms (Continued)



(a)



(b)

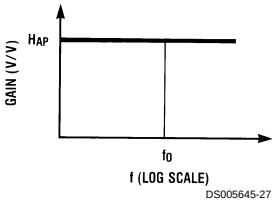
$$H_N(s) = \frac{H_{ON}(s^2 + \omega_o^2)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$Q = \frac{f_0}{f_H - f_L};\ f_0 = \sqrt{f_L f_H}$$

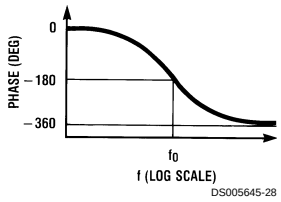
$$f_L = f_0\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_0\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 4. 2nd-Order Notch Response



(a)



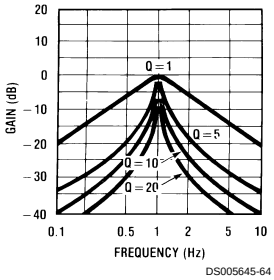
(b)

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

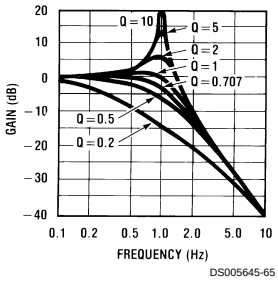
FIGURE 5. 2nd-Order All-Pass Response

1.0 Definitions of Terms (Continued)

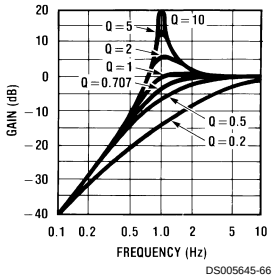
(a) Bandpass



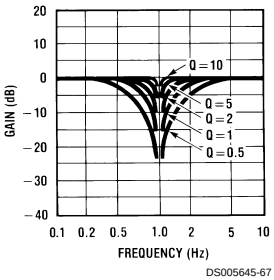
(b) Low Pass



(c) High-Pass



(d) Notch



(e) All-Pass

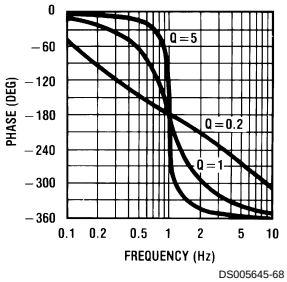


FIGURE 6. Response of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

2.0 Modes of Operation

The LMF100 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain analysis is appropriate. Since this is cumbersome, and since the LMF100 closely approximates continuous filters, the following discussion is based on the well-known frequency domain. Each LMF100 can produce two full 2nd order functions. See *Table 1* for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_0$ (See *Figure 7*)

f_0 = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_{notch} = center frequency of the imaginary zero pair = f_0.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) = $-\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_0$) = $-\frac{R3}{R1}$

H_{ON} = Notch output gain as $f \rightarrow 0$, $f \rightarrow f_{CLK}/2$ $= \frac{-R_2}{R_1}$

$Q = \frac{f_0}{BW} = \frac{R3}{R2}$

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$H_{OLP} = \frac{H_{OBP}}{Q}$ or $H_{OBP} = H_{OLP} \times Q$

$= H_{ON} \times Q.$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$f_0 = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = -1$; $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

Circuit dynamics: $H_{OBP_1} = Q$

Note: V_{IN} should be driven from a low impedance (<1 kΩ) source.

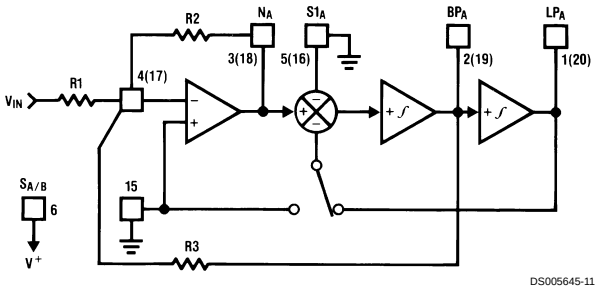


FIGURE 7. MODE 1

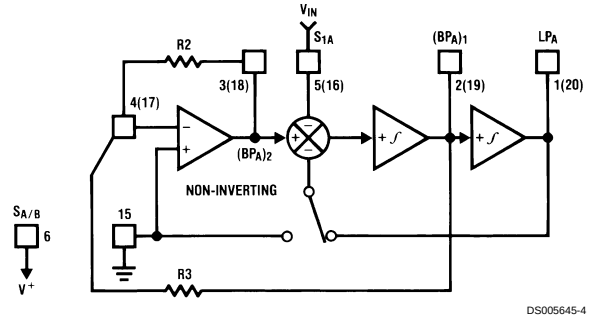


FIGURE 8. MODE 1a

2.0 Modes of Operation (Continued)

MODE 1b: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_0$ (See *Figure 9*)

f_0 = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100} \times \sqrt{2}$ or $\frac{f_{CLK}}{50} \times \sqrt{2}$

f_{notch} = center frequency of the imaginary zero pair = f_0.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R2}{2R1}$

H_{OBP} = Bandpass gain (at $f = f_0$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $\left.\begin{matrix} f \rightarrow 0 \\ f \rightarrow f_{CLK}/2 \end{matrix}\right\} = \frac{-R_2}{R_1}$

$Q = \frac{f_0}{BW} = \frac{R3}{R2} \times \sqrt{2}$

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$H_{OLP} = \frac{H_{OBP}}{\sqrt{2}\,Q}$ or $H_{OBP} = H_{OLP} \times Q \times \sqrt{2}$

$H_{OBP} = \frac{H_{ON} \times Q}{\sqrt{2}}$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_0$
(See *Figure 10*)

f_0 = center frequency

$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4} + 1}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4} + 1}$

$f_{notch} = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

Q = quality factor of the complex pole pair

$= \frac{\sqrt{R2/R4 + 1}}{R2/R3}$

H_{OLP} = Lowpass output gain (as $f \rightarrow 0$)

$= -\frac{R2/R1}{R2/R4 + 1}$

H_{OBP} = Bandpass output gain (at $f = f_0$) = − R3/R1

H_{ON_1} = Notch output gain (as $f \rightarrow 0$)

$= -\frac{R2/R1}{R2/R4 + 1}$

H_{ON_2} = Notch output gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = \sqrt{H_{ON_1}\,H_{ON_2}}$

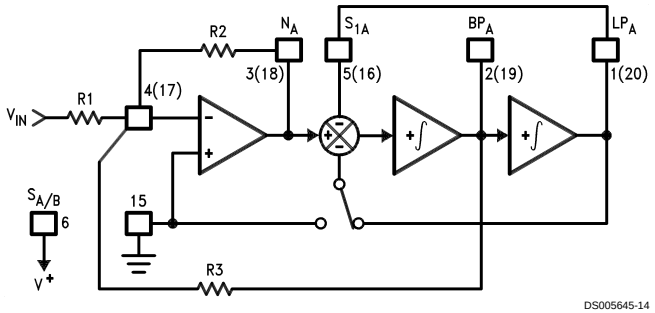


FIGURE 9. MODE 1b

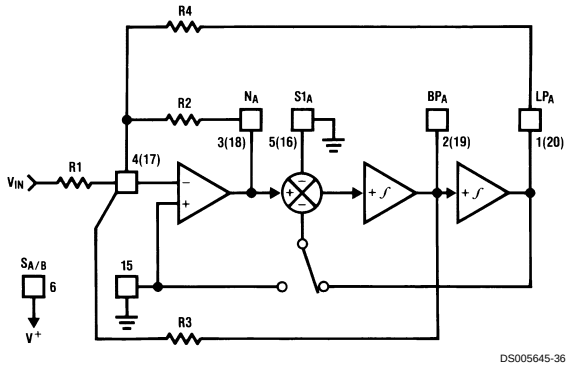


FIGURE 10. MODE 2

2.0 Modes of Operation (Continued)

MODE 3: Highpass, Bandpass, Lowpass Outputs
(See *Figure 11*)

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \text{quality factor of the complex pole pair} = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = \text{Highpass gain} \left(\text{at } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_0) = -\frac{R3}{R1}$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R4}{R1}$$

$$\text{Circuit dynamics: } \frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}};\ H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

$$H_{OHP(peak)} \cong Q \times H_{OHP} \text{ (for high Q's)}$$

MODE 3a: HP, BP, LP and Notch with External Op Amp
(See *Figure 12*)

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

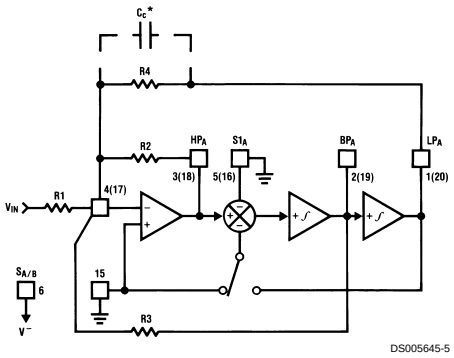
$$H_{OLP} = -\frac{R4}{R1}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100} \sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50} \sqrt{\frac{R_h}{R_l}}$$

$$H_{ON} = \text{gain of notch at } f = f_0 = \left\| Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right) \right\|$$

$$H_{n1} = \text{gain of notch (as } f \rightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{n2} = \text{gain of notch} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$$



*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF−100 pF) across R4 to provide some phase lead.

FIGURE 11. MODE 3

2.0 Modes of Operation (Continued)

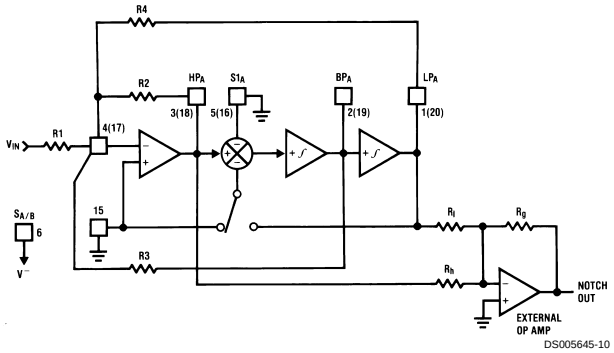


FIGURE 12. MODE 3a

MODE 4: Allpass, Bandpass, Lowpass Outputs

(See *Figure 13*)

f_0 = center frequency

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$;

f_z* = center frequency of the complex zero $\approx f_0$

$Q = \frac{f_0}{BW} = \frac{R3}{R2}$;

Q_z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

H_{OAP}* = Allpass gain $\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$)

$= -\left(\frac{R2}{R1} + 1\right) = -2$

H_{OBP} = Bandpass gain (at $f = f_0$)

$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$

Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_0 occurs causing a 0.4 dB peaking around f_0 of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

MODE 5: Numerator Complex Zeros, BP, LP

(See *Figure 14*)

$f_0 = \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{100}$ or $\sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{50}$

$f_z = \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{100}$ or $\sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{50}$

$Q = \sqrt{1 + R2/R4} \times \frac{R3}{R2}$

$Q_Z = \sqrt{1 - R1/R4} \times \frac{R3}{R1}$

H_{0z1} = gain at C.Z. output (as $f \rightarrow 0$ Hz) $= \frac{-R2(R4 - R1)}{R1(R2 + R4)}$

H_{0z2} = gain at C.Z. output $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$

$H_{OBP} = -\left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2}$

$H_{OLP} = -\left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1}$

2.0 Modes of Operation (Continued)

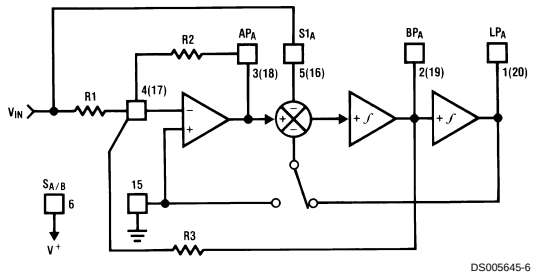


FIGURE 13. MODE 4

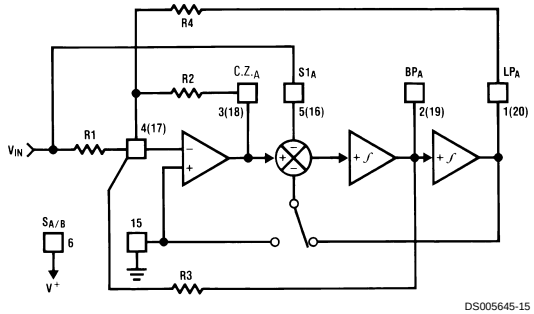


FIGURE 14. MODE 5

MODE 6a: Single Pole, HP, LP Filter (See *Figure 15*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

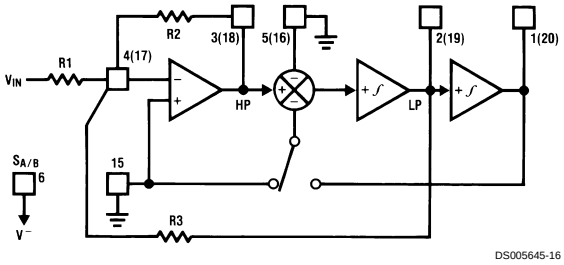


FIGURE 15. MODE 6a