DOCUMENTATION TECHNIQUE

Option B : électrotechnique

Contenu de la documentation technique :

- Circuit programmable CY7C374i
- Circuit PROM CY7C235A
- Convertisseur N/A AD7801
- Amplificateur opérationnel OP-470
- Circuits ‘mélangeur’

CY7C374i

UltraLogic™ 128-Macrocell Flash CPLD

Features

- **128 macrocells in eight logic blocks**
- **64 I/O pins**
- **5 dedicated inputs including 4 clock pins**
- **In-System Reprogrammable™ (ISR™) Flash technology**
  - **JTAG interface**
- **Bus Hold capabilities on all I/Os and dedicated inputs**
- **No hidden delays**
- **High speed**
  - **f_{MAX} = 125 MHz**
  - **t_{PD} = 10 ns**
  - **t_S = 5.5 ns**
  - **t_{CO} = 6.5 ns**
- **Fully PCI compliant**
- **3.3V or 5.0V I/O operation**
- **Available in 84-pin PLCC, 84-pin CLCC, and 100-pin TQFP packages**
- **Pin compatible with the CY7C373i**

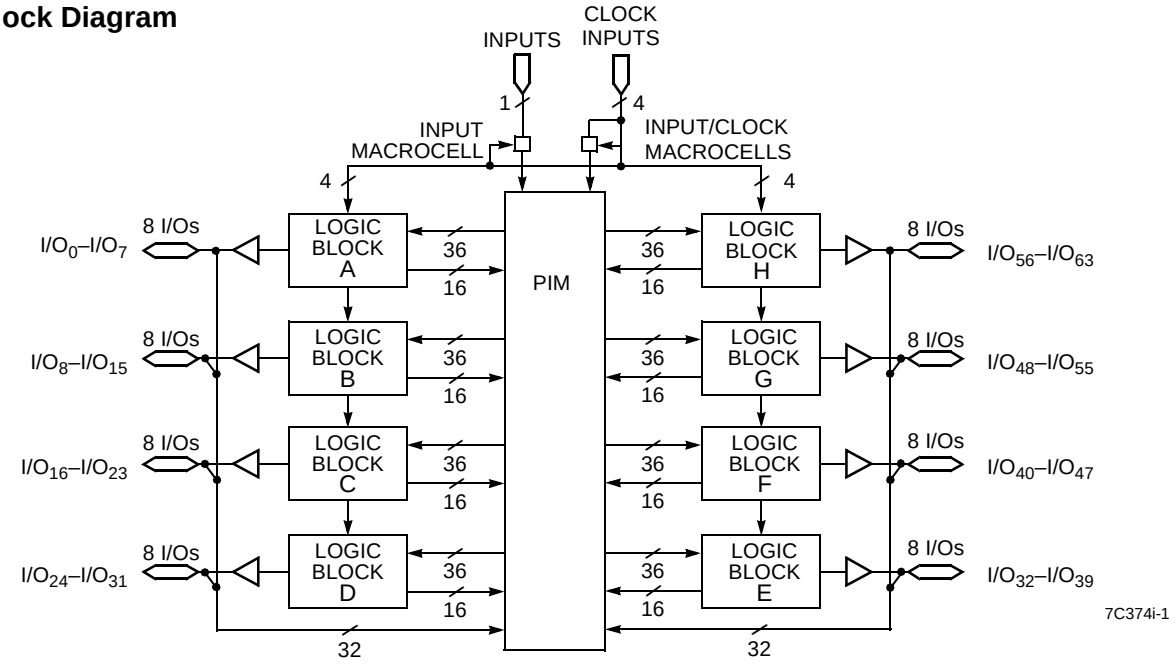
Functional Description

The CY7C374i is an In-System Reprogrammable Complex Programmable Logic Device (CPLD) and is part of the FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C374i is designed to bring the ease of use as well as PCI Local Bus Specification support and high performance of the 22V10 to high-density CPLDs.

Like all of the UltraLogic™ FLASH370i devices, the CY7C374i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The Cypress ISR function is implemented through a JTAG serial interface. Data is shifted in and out through the SDI and SDO pin. The ISR interface is enabled using the programming voltage pin (ISR_{EN}). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 128 macrocells in the CY7C374i are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

Logic Block Diagram



Selection Guide

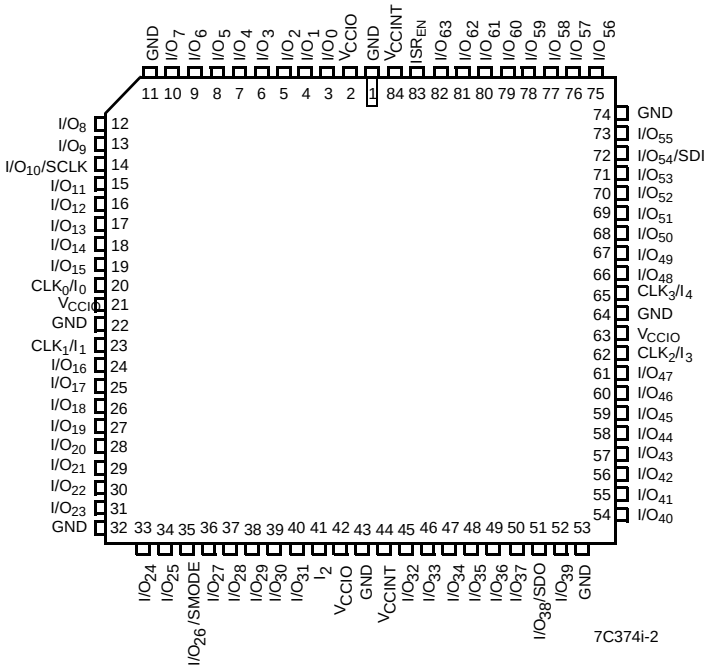
	7C374i–125	7C374i–100	7C374i–83	7C7374iL–83	7C374i–66	7C374iL–66
Maximum Propagation Delay[1], t_{PD} (ns)	10	12	15	15	20	20
Minimum Set-Up, t_S (ns)	5.5	6	8	8	10	10
Maximum Clock to Output[1], t_{CO} (ns)	6.5	7	8	8	10	10
Typical Supply Current, I_{CC} (mA)	125	125	125	75	125	75

Note:

1. The 3.3V I/O mode timing adder, $t_{3.3IO}$, must be added to this specification when V_{CCIO} = 3.3V.

Pin Configurations

PLCC
Top View



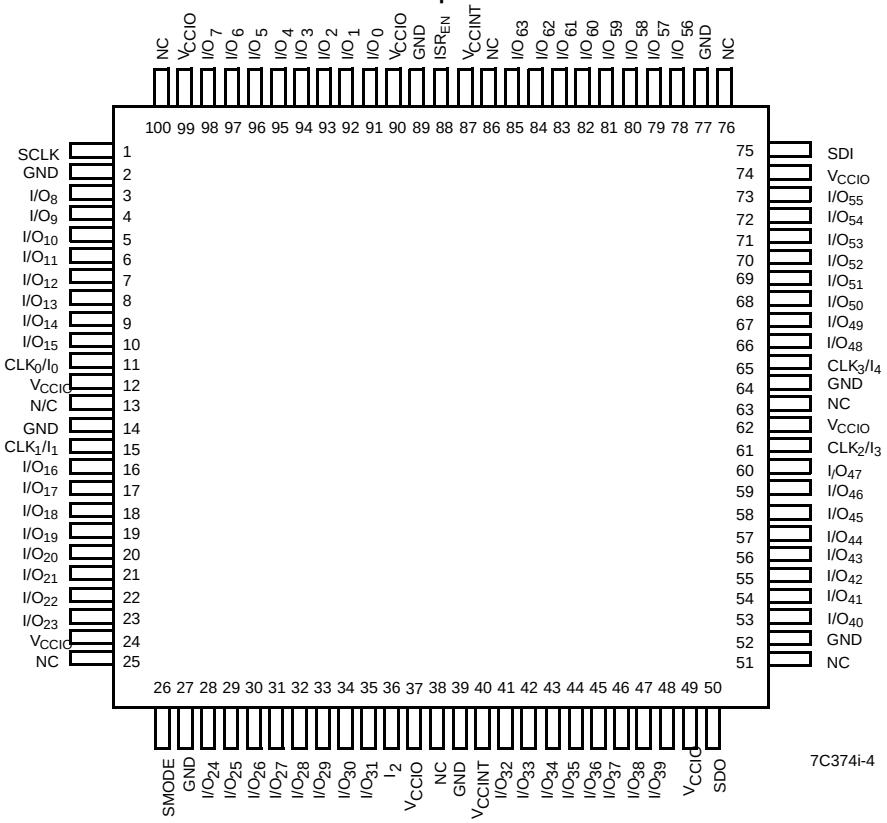
PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L	I/O_{23}	I/O_{25}	I/O_{26} SMODE	I/O_{28}	I/O_{31}	I/O_{33}	V_{CC}	I/O_{34}	I/O_{36}	I/O_{37}	I/O_{39}
K	I/O_{21}	GND	I/O_{24}	I/O_{27}	I/O_{30}	I_2	I/O_{32}	I/O_{35}	I/O_{38} SDO	GND	I/O_{41}
J	I/O_{20}	I/O_{22}			I/O_{29}	V_{CC}	GND			I/O_{40}	I/O_{42}
H	I/O_{18}	I/O_{19}								I/O_{43}	I/O_{44}
G	CLK1 /I_1	I/O_{16}	GND						CLK2 /I_3	I/O_{46}	I/O_{47}
F	I/O_{17}	CLK0 /I_0	V_{CC}						V_{CC}	I/O_{45}	GND
E	I/O_{15}	I/O_{14}	I/O_{13}						I/O_{49}	I/O_{48}	CLK3 /I_4
D	I/O_{12}	I/O_{11}								I/O_{51}	I/O_{50}
C	I/O_{10} SCLK	I/O_8	■		I/O_1	V_{CC}	ISR_{EN}			I/O_{54} SDI	I/O_{52}
B	I/O_9	GND	I/O_6	I/O_3	I/O_0	I/O_{61}	I/O_{62}	I/O_{59}	I/O_{56}	GND	I/O_{53}
A	I/O_7	I/O_5	I/O_4	I/O_2	V_{CC}	GND	I/O_{63}	I/O_{60}	I/O_{58}	I/O_{57}	I/O_{55}

7C374i–3

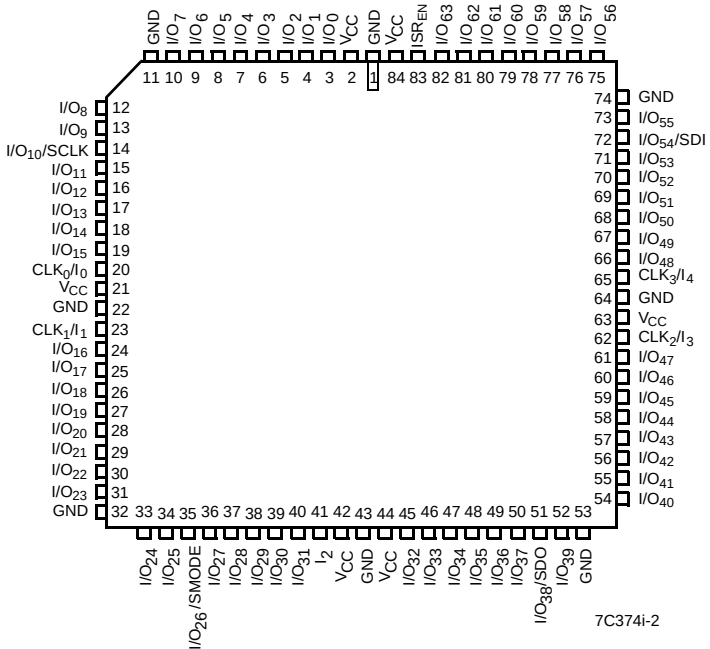
Pin Configurations (continued)

TQFP
Top View



7C374i-4

CLCC
Top View



7C374i-2

Functional Description (continued)

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370i family, the CY7C374i is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374i. In addition, there is one dedicated input and four input/clock pins.

Finally, the CY7C374i features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C374i remain the same.

Logic Block

The number of logic blocks distinguishes the members of the FLASH370i family. The CY7C374i includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370i logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370i CPLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C374i have I/O pins associated with them. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The I/O macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C374i to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Programming

For an overview of ISR programming, refer to the FLASH370i Family data sheet and for ISR cable and software specifications, refer to ISR data sheets. For a detailed description of ISR capabilities, refer to the Cypress application note, “An Introduction to In System Reprogramming with FLASH370i.”

PCI Compliance

The FLASH370i family of CMOS CPLDs are fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The simple and predictable timing model of FLASH370i ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without simple and predictable timing, PCI compliance is dependent upon routing and product term distribution.

3.3V or 5.0V I/O Operation

The FLASH370i family can be configured to operate in both 3.3V and 5.0V systems. All devices have two sets of V_{CC} pins: one set, V_{CCINT}, for internal operation and input buffers, and another set, V_{CCIO}, for I/O output drivers. V_{CCINT} pins must always be connected to a 5.0V power supply. However, the V_{CCIO} pins may be connected to either a 3.3V or 5.0V power supply, depending on the output requirements. When V_{CCIO} pins are connected to a 5.0V source, the I/O voltage levels are compatible with 5.0V systems. When V_{CCIO} pins are connected to a 3.3V source, the input voltage levels are compatible with both 5.0V and 3.3V systems, while the output voltage levels are compatible with 3.3V systems. There will be an additional timing delay on all output buffers when operating in 3.3V I/O mode. The added flexibility of 3.3V I/O capability is available in commercial and industrial temperature ranges.

Bus Hold Capabilities on all I/Os and Dedicated Inputs

In addition to ISR capability, a new feature called bus-hold has been added to all FLASH370i I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device’s performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Design Tools

Development software for the CY7C371i is available from Cypress’s *Warp*™, *Warp* Professional™, and *Warp* Enterprise™ software packages. Please refer to the data sheets on these products for more details. Cypress also actively supports almost all third-party design tools. Please refer to third-party tool support for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage..... –0.5V to +7.0V

DC Program Voltage.....12.5V

Output Current into Outputs.....16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC} V_{CCINT}	V_{CCIO}
Commercial	0°C to +70°C	5V ± 0.25V	5V ± 0.25V OR 3.3V ± 0.3V
Industrial	–40°C to +85°C	5V ± 0.5V	5V ± 0.5V OR 3.3V ± 0.3V
Military[2]	–55°C to +125°C	5V ± 0.5V	

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[5]	2.4			V
			I_{OH} = –2.0 mA (Mil)				V
V_{OHZ}	Output HIGH Voltage with Output Disabled[9]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l/Ind)[5, 6]			4.0	V
			I_{OH} = –50 µA (Com'l/Ind)[5, 6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[5]			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[7]		2.0		7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = Internal GND, V_I = V_{CC}		–10		+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_O = GND or V_O = V_{CC}, Output Disabled		–50		+50	µA
		V_{CC} = Max., V_O = 3.3V, Output Disabled[6]		0	–70	–125	µA
I_{OS}	Output Short Circuit Current[8, 9]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = 1 MHz, V_{IN} = GND, V_{CC}[10]	Com'l/Ind.		125	200	mA
			Com'l "L" –66		75	125	mA
			Military		125	250	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Notes:

2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. If V_{CCIO} is not specified, the device can be operating in either 3.3V or 5V I/O mode; V_{CC}=V_{CCINT}.
5. I_{OH} = –2 mA, I_{OL} = 2 mA for SDO.
6. When the I/O is three-stated, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are three-stated during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Measured with 16-bit counter programmed into each logic block.

Capacitance[9]

Parameter	Description	Test Conditions	Min.	Max.	Unit
$C_{I/O}$[11, 12]	Input Capacitance	V_{IN} = 5.0V at f = 1 MHz		8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz	5	12	pF

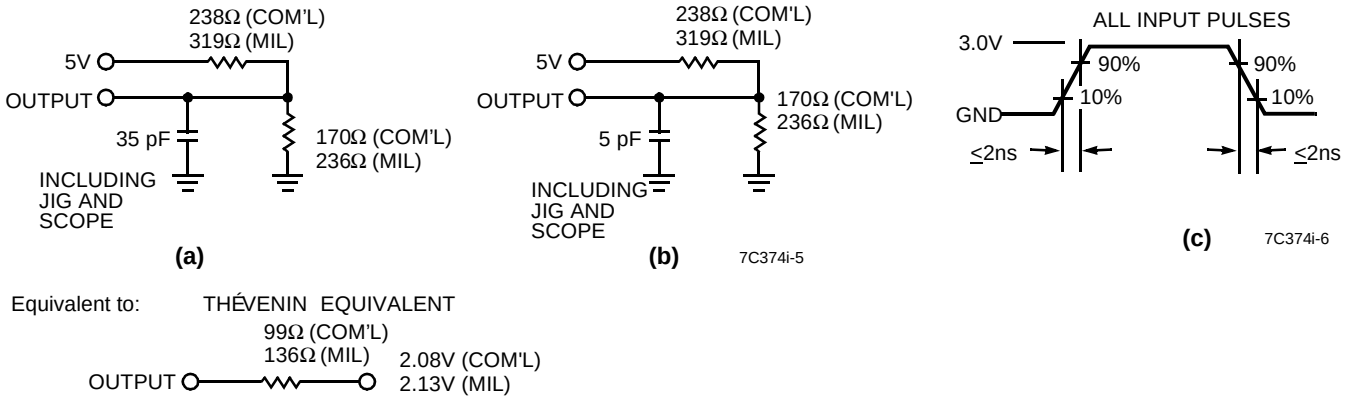
Inductance[9]

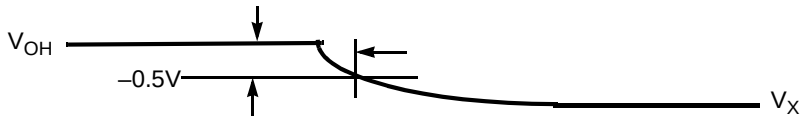
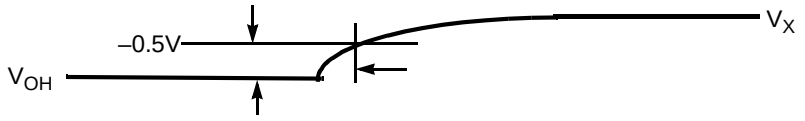
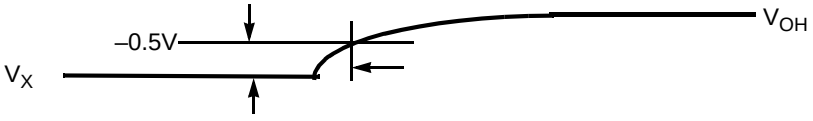
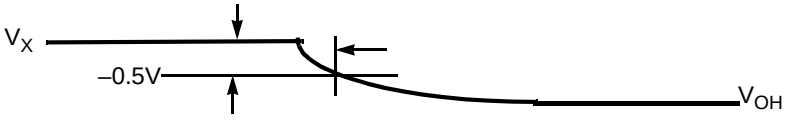
Parameter	Description	Test Conditions	100-PinTQFP	84-Lead PLCC	84-Lead CLCC	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	8	8	5	nH

Endurance Characteristics[9]

Parameter	Description	Test Conditions	Max.	Unit
N	Maximum Reprogramming Cycles	Normal Programming Conditions	100	Cycles

AC Test Loads and Waveforms



Parameter[13]	V_X	Output Waveform Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{thc}	

Notes:
11. $C_{I/O}$ for the CLCC package are 12 pF Max
12. $C_{I/O}$ for dedicated Inputs, and for I/O pins with JTAG functionality is 12 pF Max., and for ISR_{EN} is 15 pF Max.
13. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[14]

Parameter	Description	7C374i–125		7C374i–100		7C374i–83 7C374iL–83		7C374i–66 7C374iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output[1]		10		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch[1]		13		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches[1]		15		16		19		24	ns
t_{EA}	Input to Output Enable[1]		14		16		19		24	ns
t_{ER}	Input to Output Disable		14		16		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[9]	3		3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[9]	3		3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output[1]		14		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch[1]		16		18		21		26	ns
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output[1]		6.5		7		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	5.5		6		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)[1]		14		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	8		10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	10		12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[9]	125		100		83		66		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	158.3		143		125		100		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	83.3		76.9		67.5		50		MHz
t_{OH}–t_{IH} 37x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C37x[9, 15]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	8		10		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	125		100		83.3		66.6		MHz

Notes:

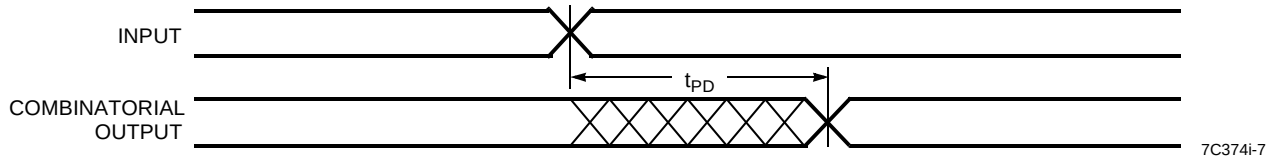
14. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
15. This specification is intended to guarantee interface compatibility of the other members of the CY7C370i family with the CY7C374i. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

Switching Characteristics Over the Operating Range[14] (continued)

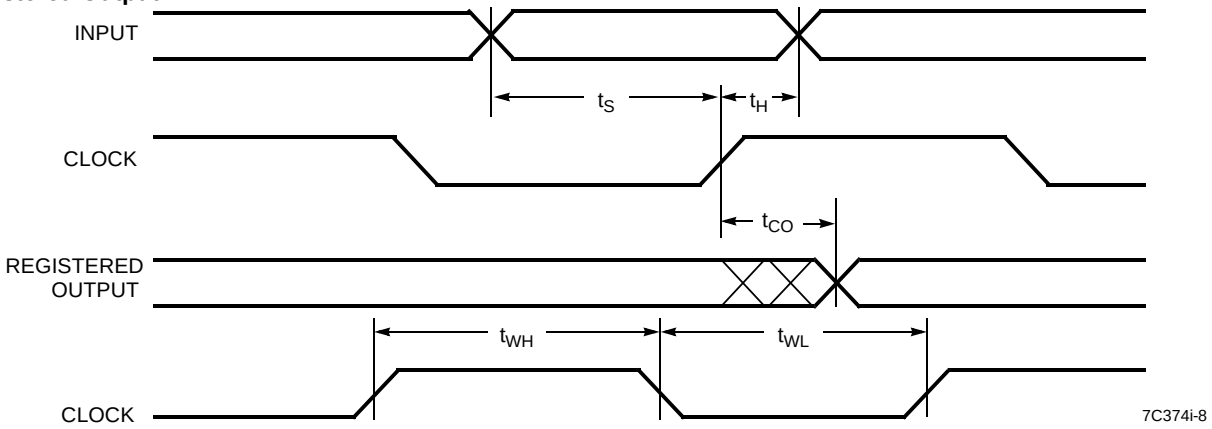
Parameter	Description	7C374i–125		7C374i–100		7C374i–83 7C374iL–83		7C374i–66 7C374iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[9]	10		12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[9]	12		14		17		22		ns
t_{RO}	Asynchronous Reset to Output[1]		16		18		21		26	ns
t_{PW}	Asynchronous Preset Width[9]	10		12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[9]	12		14		17		22		ns
t_{PO}	Asynchronous Preset to Output[1]		16		18		21		26	ns
Tap Controller Parameter										
f_{TAP}	Tap Controller Frequency	500		500		500		500		kHz
3.3V I/O Mode Parameters										
$t_{3.3IO}$	3.3V I/O mode timing adder		1		1		1		1	ns

Switching Waveforms

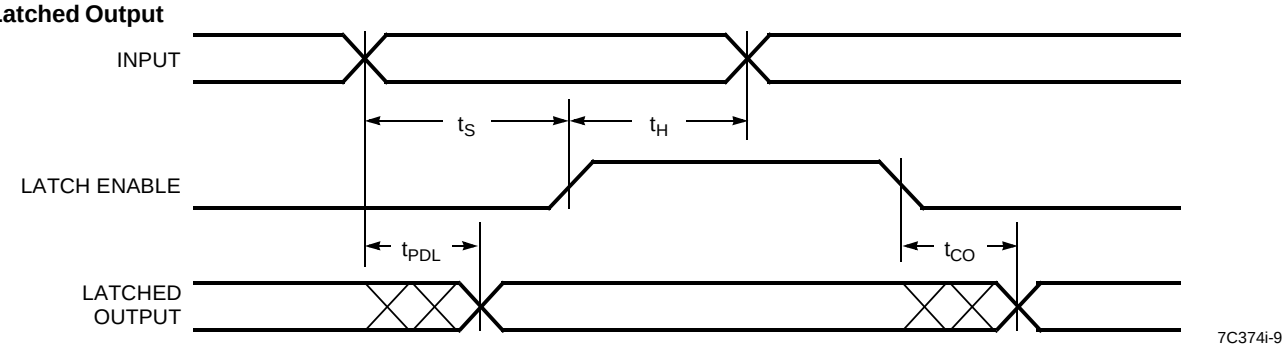
Combinatorial Output



Registered Output

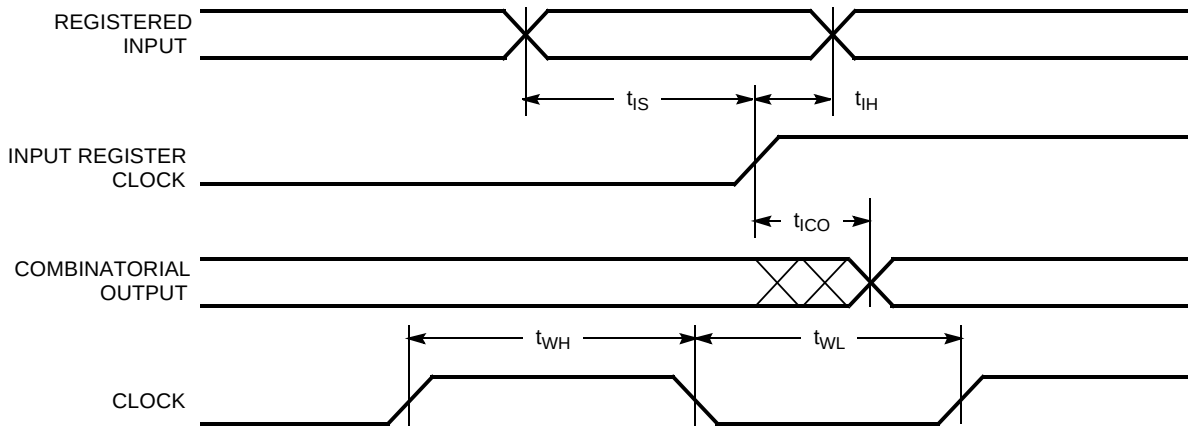


Latched Output

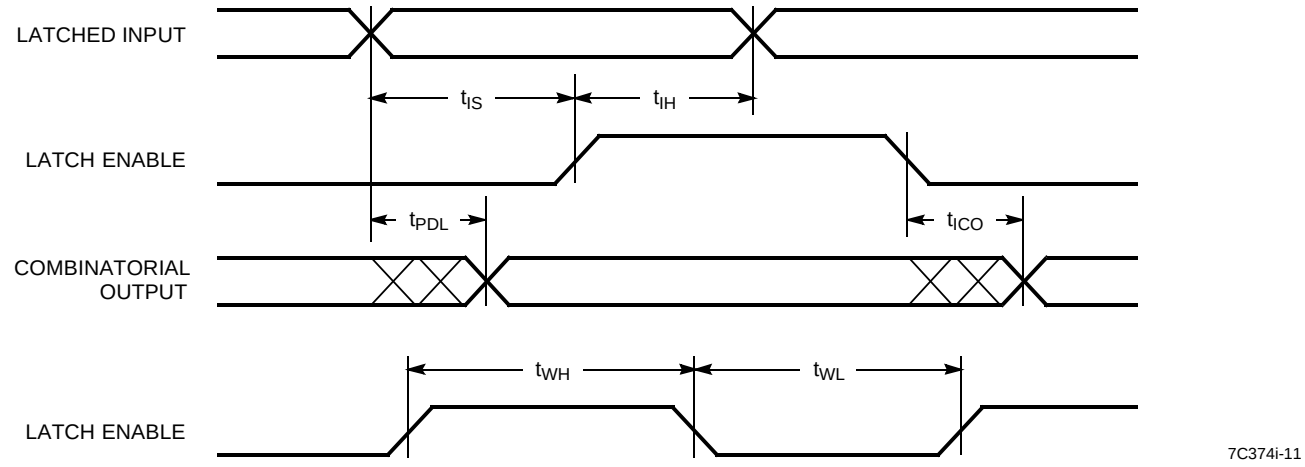


Switching Waveforms (continued)

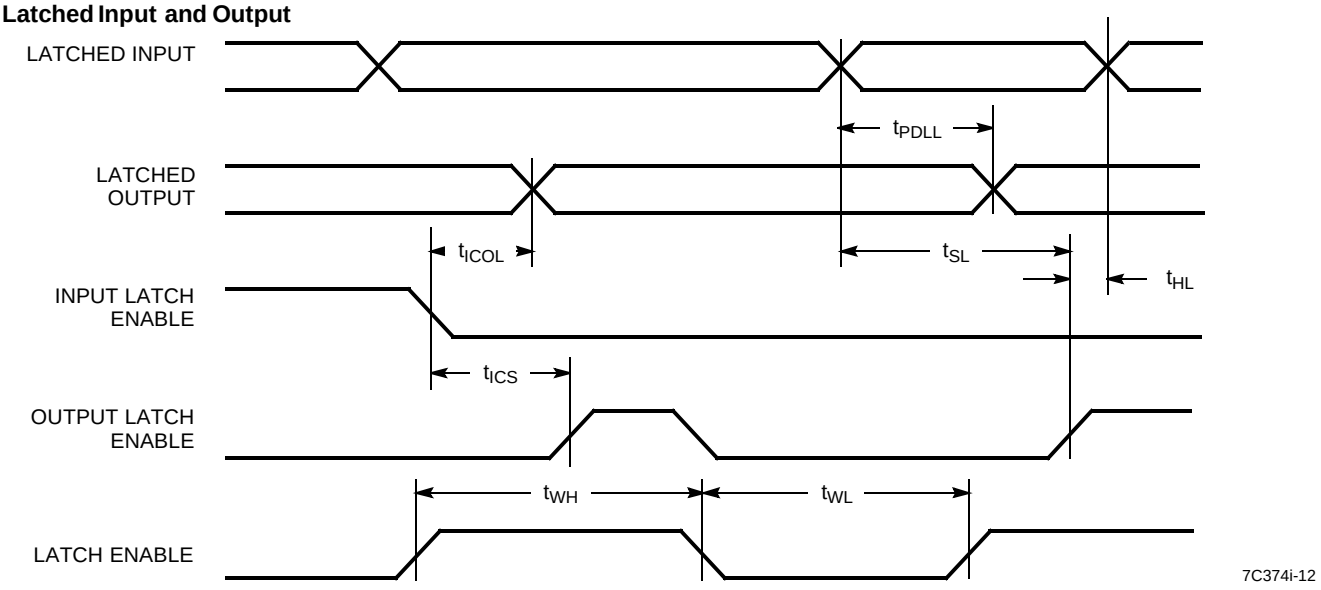
Registered Input



Latched Input

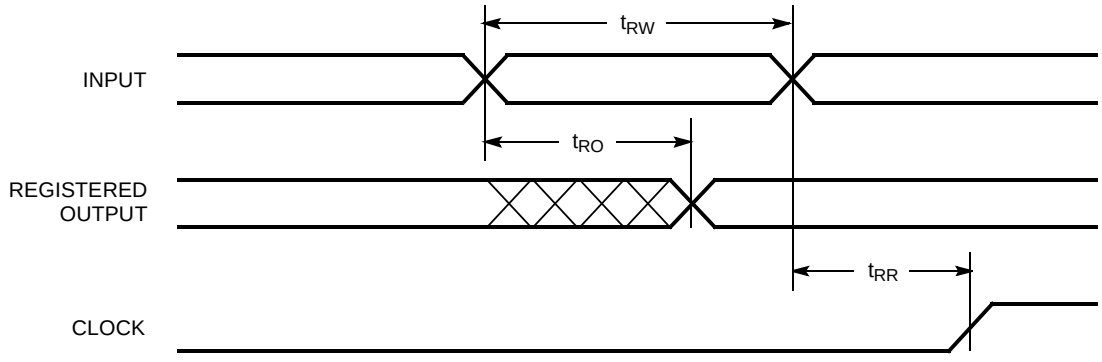


Latched Input and Output

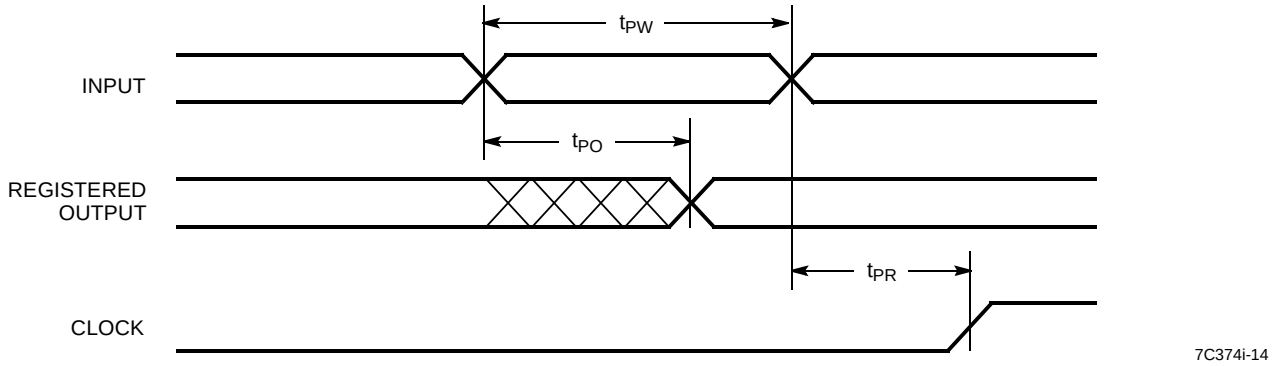


Switching Waveforms (continued)

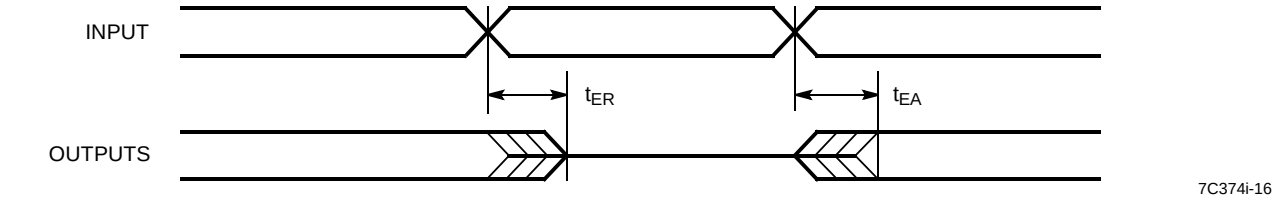
Asynchronous Reset



Asynchronous Preset



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
125	CY7C374i–125AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–125JC	J83	84-Lead Plastic Leaded Chip Carrier	
100	CY7C374i–100AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–100JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–100AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374i–100JI	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C374i–83AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–83AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374i–83JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–83GMB	G84	84-Pin Ceramic Pin Grid Array	Military
	CY7C374i–83YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
	CY7C374iL–83AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374iL–83JC	J83	84-Lead Plastic Leaded Chip Carrier	
66	CY7C374i–66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–66AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374i–66JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–66GMB	G84	84-Pin Ceramic Pin Grid Array	Military
	CY7C374i–66YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
	CY7C374iL–66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374iL–66JC	J83	84-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

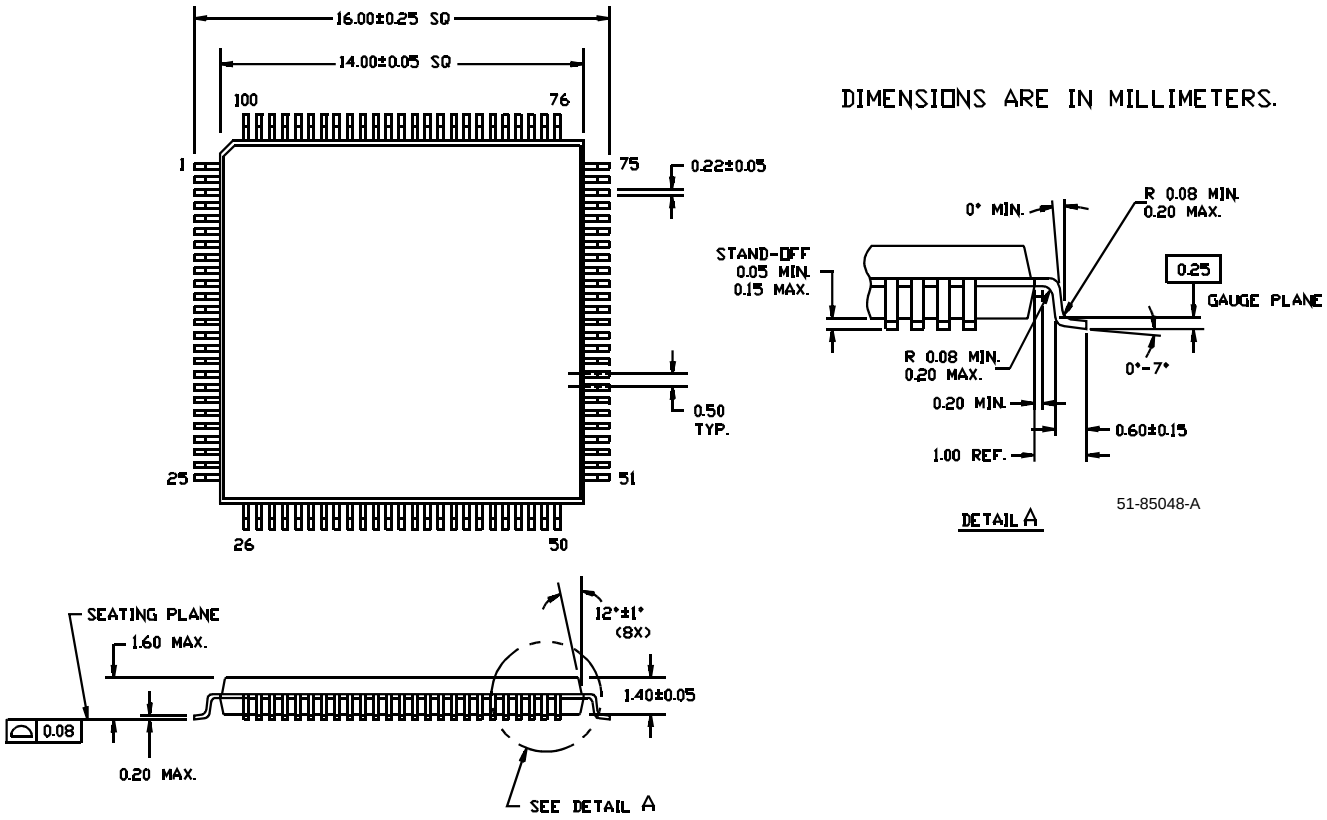
Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PDL}	9, 10, 11
t_{PDLL}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_{ICOL}	9, 10, 11
t_{S}	9, 10, 11
t_{SL}	9, 10, 11
t_{H}	9, 10, 11
t_{HL}	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11
t_{EA}	9, 10, 11
t_{ER}	9, 10, 11

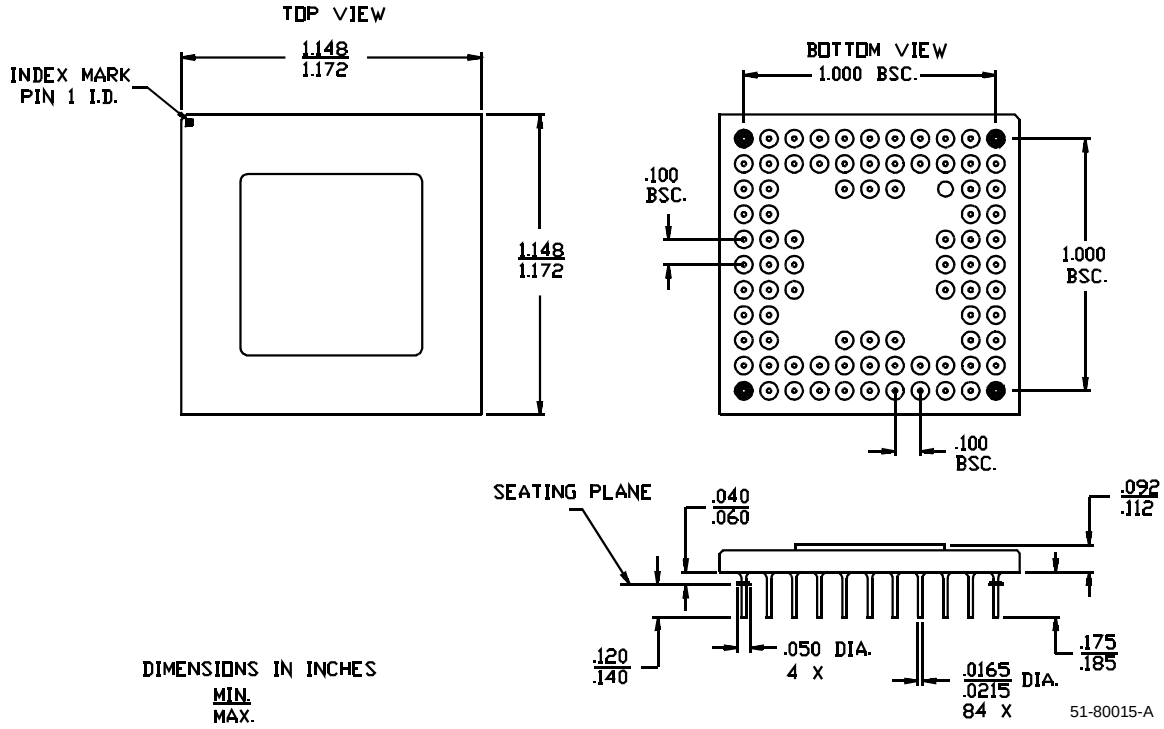
Package Diagrams

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100

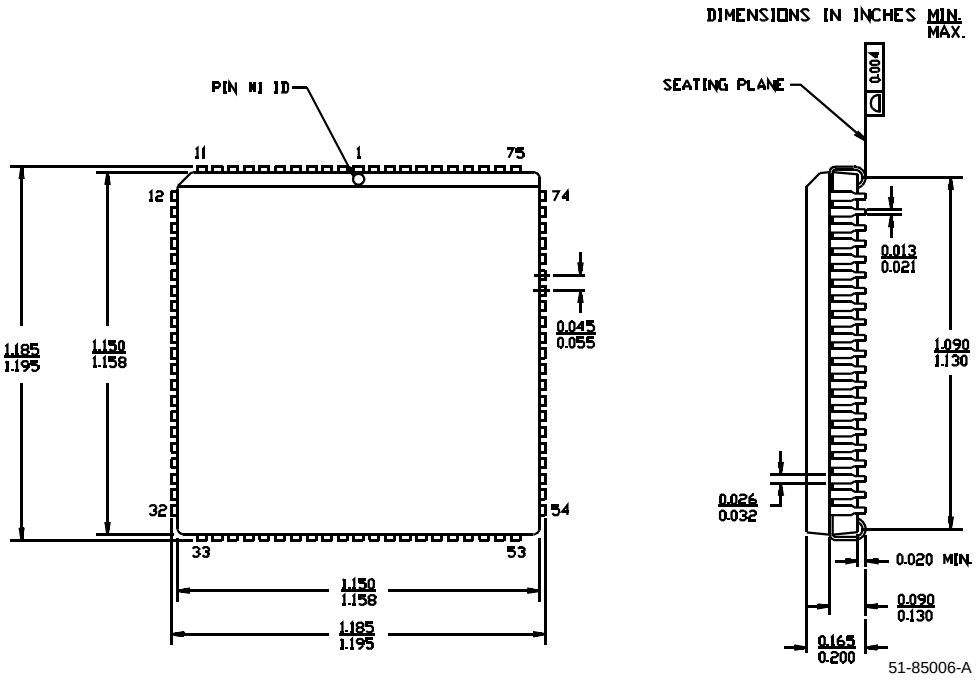


Package Diagrams (continued)

84-Pin Grid Array (Cavity Up) G84

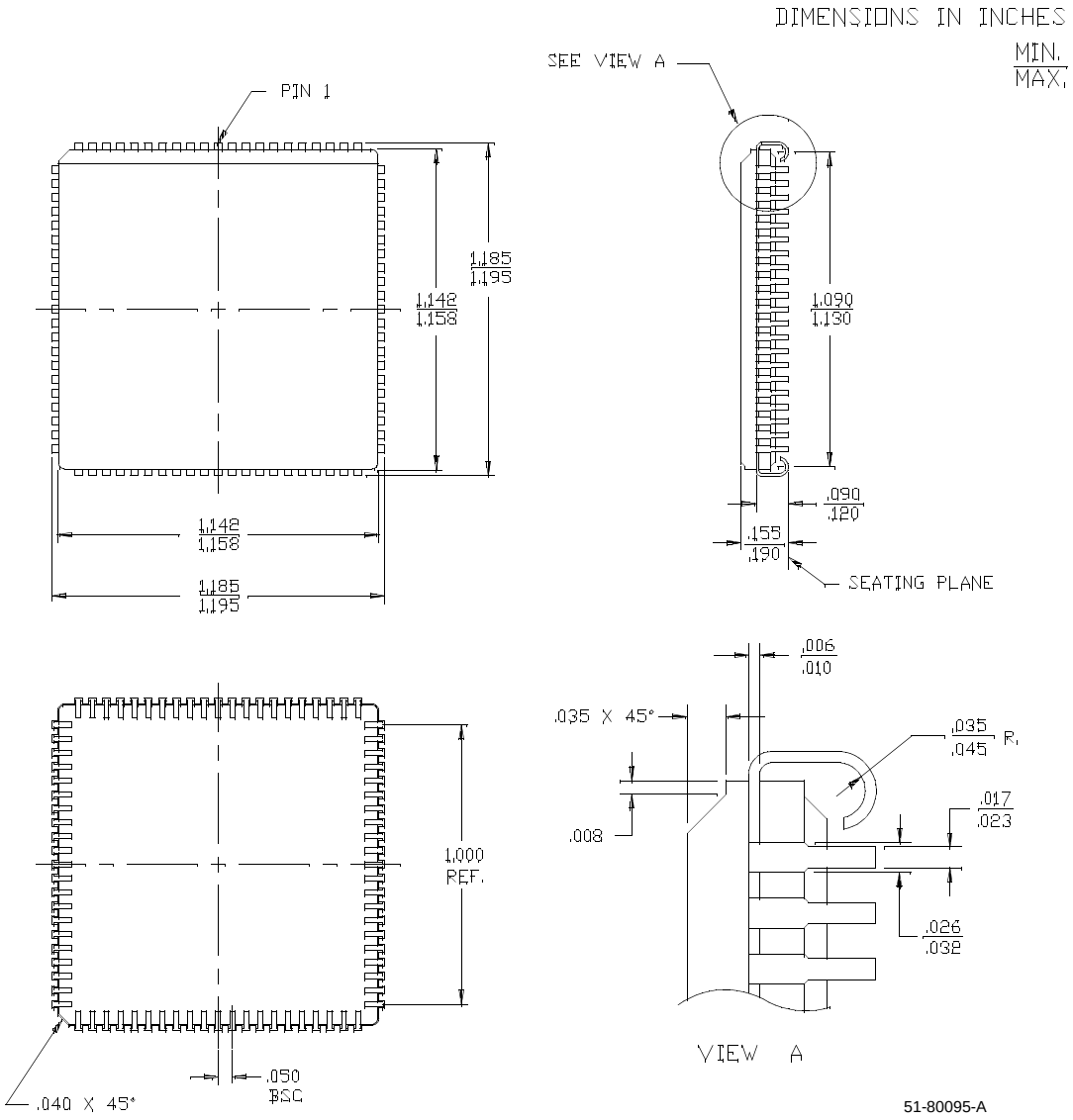


84-Lead Plastic Leaded Chip Carrier J83



Package Diagrams (continued)

84-Pin Ceramic Leaded Chip Carrier Y84



ISR, UltraLogic, FLASH370, FLASH370i, *Warp*, *Warp* Professional, and *Warp* Enterprise are trademarks of Cypress Semiconductor Corporation.

Document Title: cy7c374iUltraLogic™ 128-Macrocell Flash CPLD Document Number: 38-03031				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106376	07/11/01	SZV	Change from Spec number: 38-00496 to 38-03031

CY7C235A

1K x 8 Registered PROM

Features

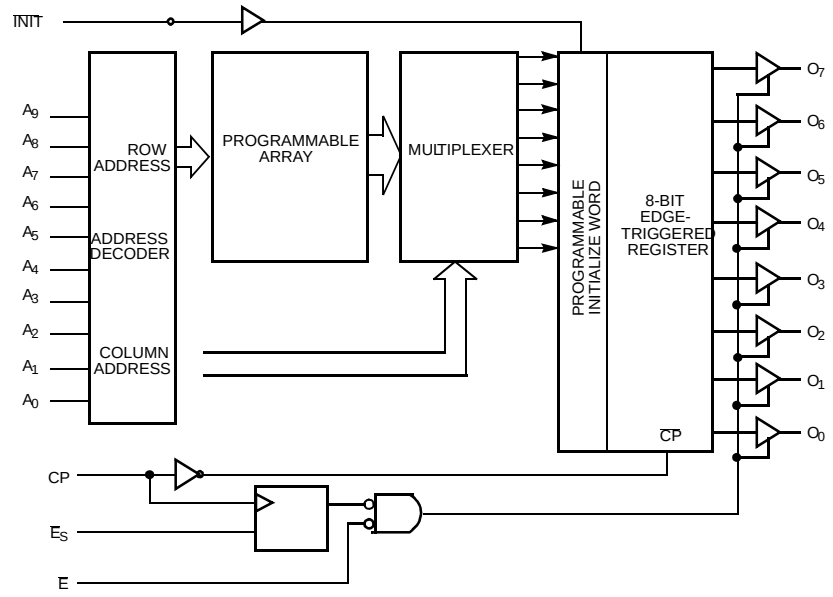
- **CMOS for optimum speed/power**
- **High speed**
  - **— 18 ns address set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Programmable asynchronous registers ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300-mil, 24-pin plastic or hermetic DIP or 28-pin LCC and PLCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

The CY7C235A is a high-performance 1024 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, or 28-pin plastic leaded chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

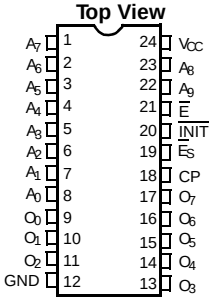
The CY7C235A replaces bipolar devices pin for pin and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage, and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet AC specification limits after customer programming.

Logic Block Diagram

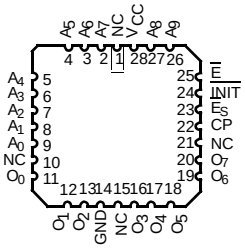


Pin Configuration

DIP
Top View



LCC/PLCC
Top View



Selection Guide

		7C235A-18	7C235A-25	7C235A-30	7C235A-40
Minimum Address Set-Up Time (ns)		18	25	30	40
Maximum Clock to Output (ns)		12	12	15	20
Maximum Operating Current (mA)	Commercial	90	90	90	90
	Military		120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12 for DIP)..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage ..... –3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20 for DIP) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	–40°C to +85°C	5V ±10%
Military[2]	–55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[3]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	µA
V_{CD}	Input Clamp Diode Voltage	Note 5				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled[4]		–10	+10	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		–20	–90	mA
I_{CC}	Power Supply Current	I_{OUT} = 0 mA, V_{CC} = Max.	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

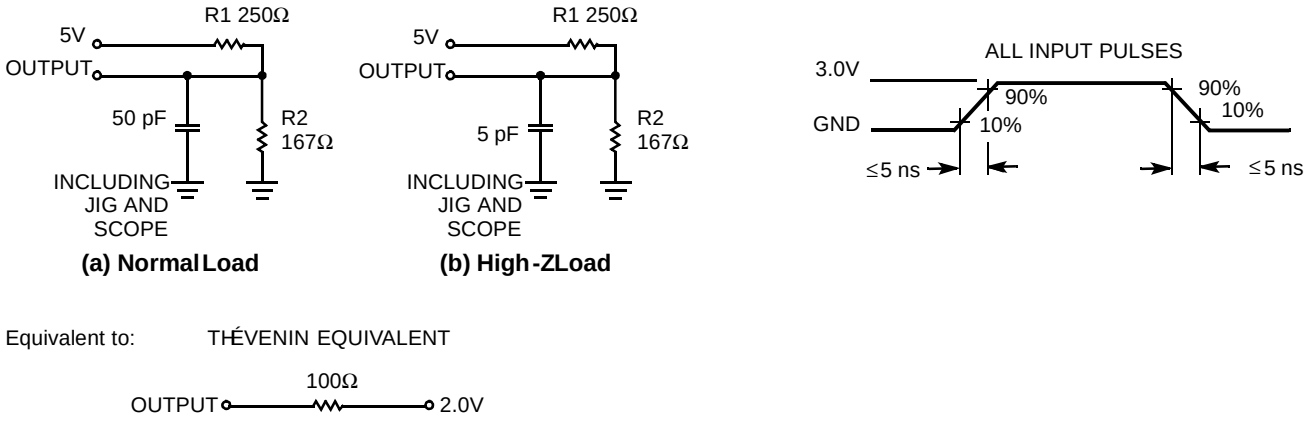
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} =5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms[5]



Operating Modes

The CY7C235A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and asynchronous initialization ($\overline{INIT}$).

Upon power-up, the synchronous enable ($\overline{E}S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address input ($A_0 - A_9$) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$), provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C235A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235A has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in “jump start” address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E}S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

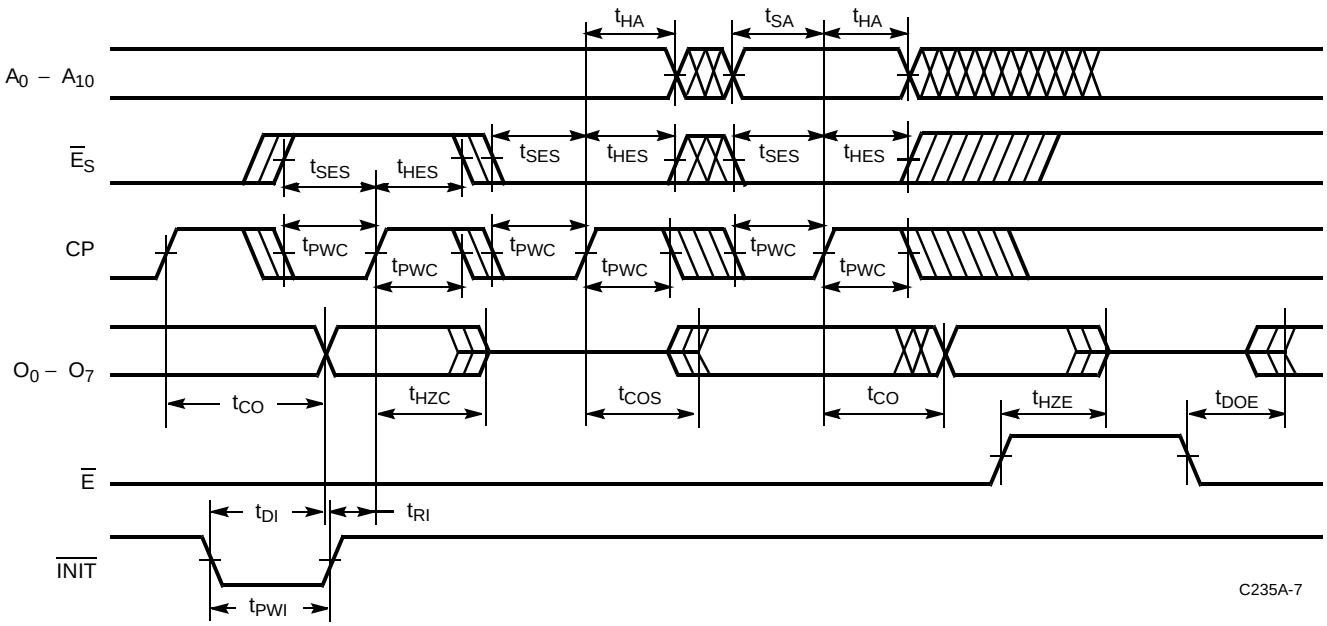
When the asynchronous initialize input, $\overline{INIT}$, is LOW, the data in the initialize byte will be asynchronously loaded into the output register. It will not, however, appear on the output pins until they are enabled, as described in the preceding paragraph.

Switching Characteristics Over Operating Range[3, 5]

Parameter	Description	7C235A-18		7C235A-25		7C235A-30		7C235A-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	18		25		30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		12		15		20	ns
t_{PWC}	Clock Pulse Width	12		12		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		10		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		20		25		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	15		20		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	15		20		20		25		ns
t_{COS}	Inactive to Valid Output from Clock HIGH[7]		15		20		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		20		20		25	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		15		20		20		25	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		15		20		20		25	ns

Note:
7. Applies only when the synchronous ($\overline{E}_S$) function is used.

Switching Waveforms[5]



Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[8]							
	Read or Output Disable	**A_0, A_3 – A_9**	**A_1**	**A_2**	**CP**	**$\overline{E_S}$**	**E**	**$\overline{INIT}$**	**O_7 – O_0**
	Other	**A_0, A_3 – A_9**	**A_1**	**A_2**	**$\overline{PGM}$**	**$\overline{VFY}$**	**E**	**V_{PP}**	**D_7 – D_0**
Read		A_0, A_3 – A_9	A_1	A_2	X	V_{IL}	V_{IL}	V_{IH}	O_7 – O_0
Output Disable		A_0, A_3 – A_9	A_1	A_2	X	V_{IH}	X	V_{IH}	High Z
Output Disable		A_0, A_3 – A_9	A_1	A_2	X	X	V_{IH}	V_{IH}	High Z
Initialize		A_0, A_3 – A_9	A_1	A_2	X	X	V_{IL}	V_{IL}	Init Byte
Program		A_0, A_3 – A_9	A_1	A_2	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	D_7 – D_0
Program Verify		A_0, A_3 – A_9	A_1	A_2	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	O_7 – O_0
Program Inhibit		A_0, A_3 – A_9	A_1	A_2	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		A_0, A_3 – A_9	A_1	A_2	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	D_7 – D_0
Program Initialize Byte		A_0, A_3 – A_9	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	D_7 – D_0
Blank Check		A_0, A_3 – A_9	A_1	A_2	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	Zeros

Note:
8. X = “don’t care” but not to exceed V_{CC} ±5%.

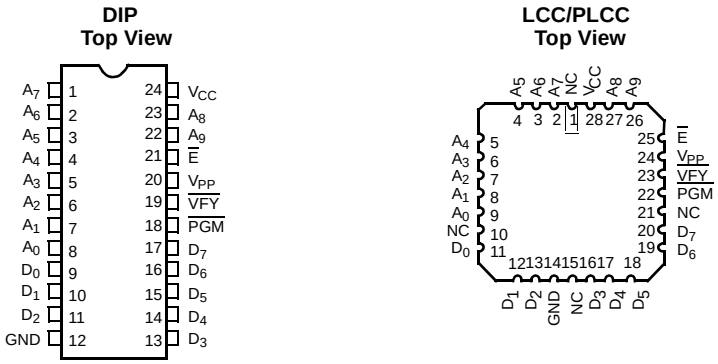
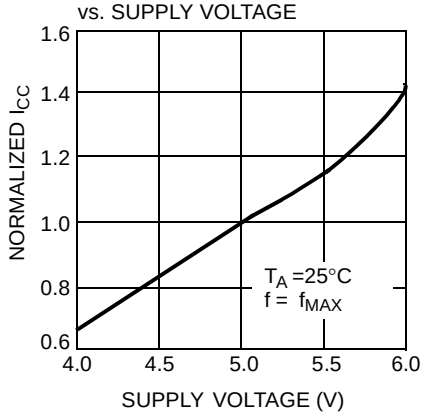


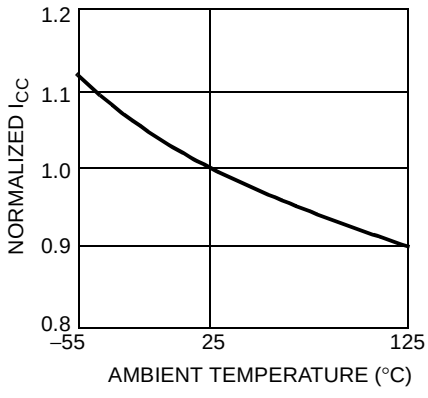
Figure 1. Programming Pinouts.

Typical DC and AC Characteristics

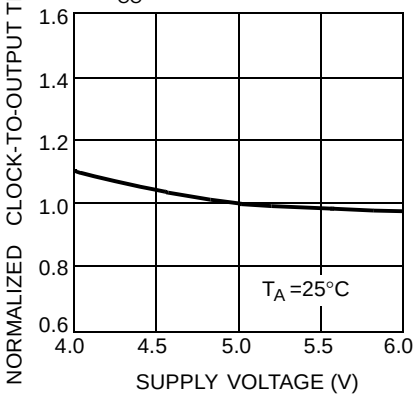
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



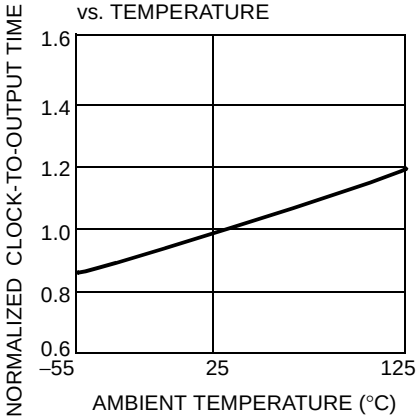
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



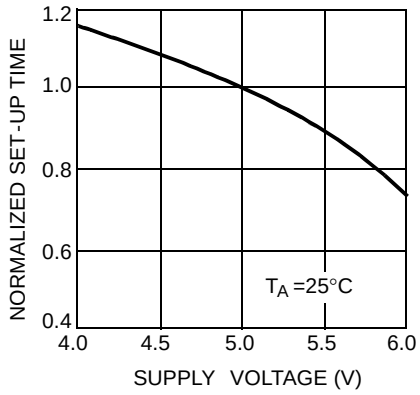
CLOCK TO OUTPUT TIME vs. V_{CC}



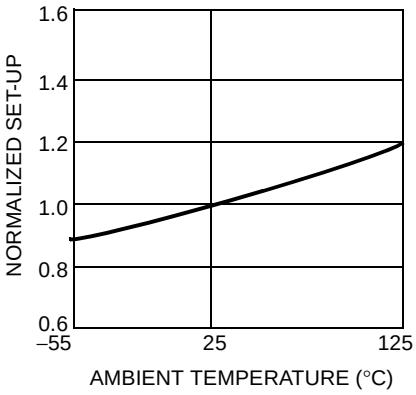
CLOCK TO OUTPUT TIME vs. TEMPERATURE



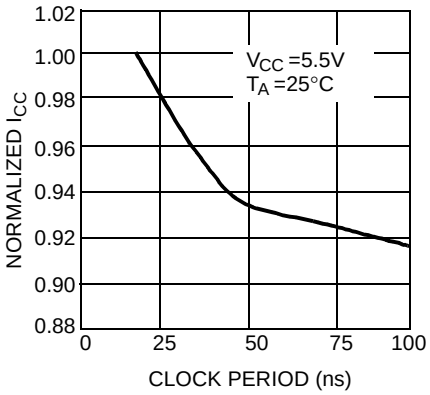
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



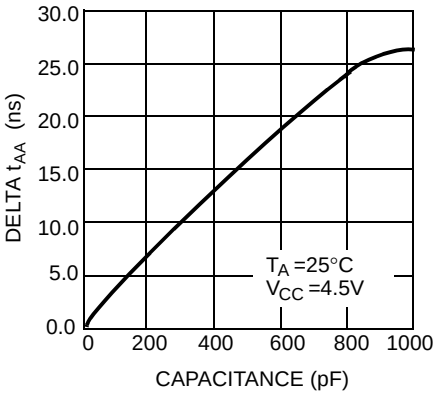
NORMALIZED SET-UP TIME vs. TEMPERATURE



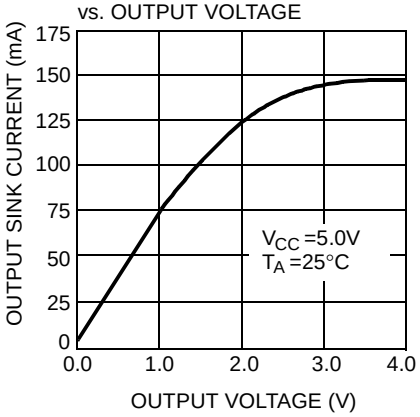
NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C235A-10

Ordering Information[9]

Speed (ns)		Ordering Code	Package Name	Package Type	Operating Range
t_{SA}	t_{CO}				
18	12	CY7C235A-18DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A-18JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A-18PC	P13	24-Lead (300-Mil) Molded DIP	
25	12	CY7C235A-25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A-25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A-25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A-25LMB	L64	28-Square Leadless Chip Carrier	
30	15	CY7C235A-30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A-30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A-30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A-30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A-30LMB	L64	28-Square Leadless Chip Carrier	
40	20	CY7C235A-40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A-40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A-40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A-40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A-40LMB	L64	28-Square Leadless Chip Carrier	

Note:

9. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

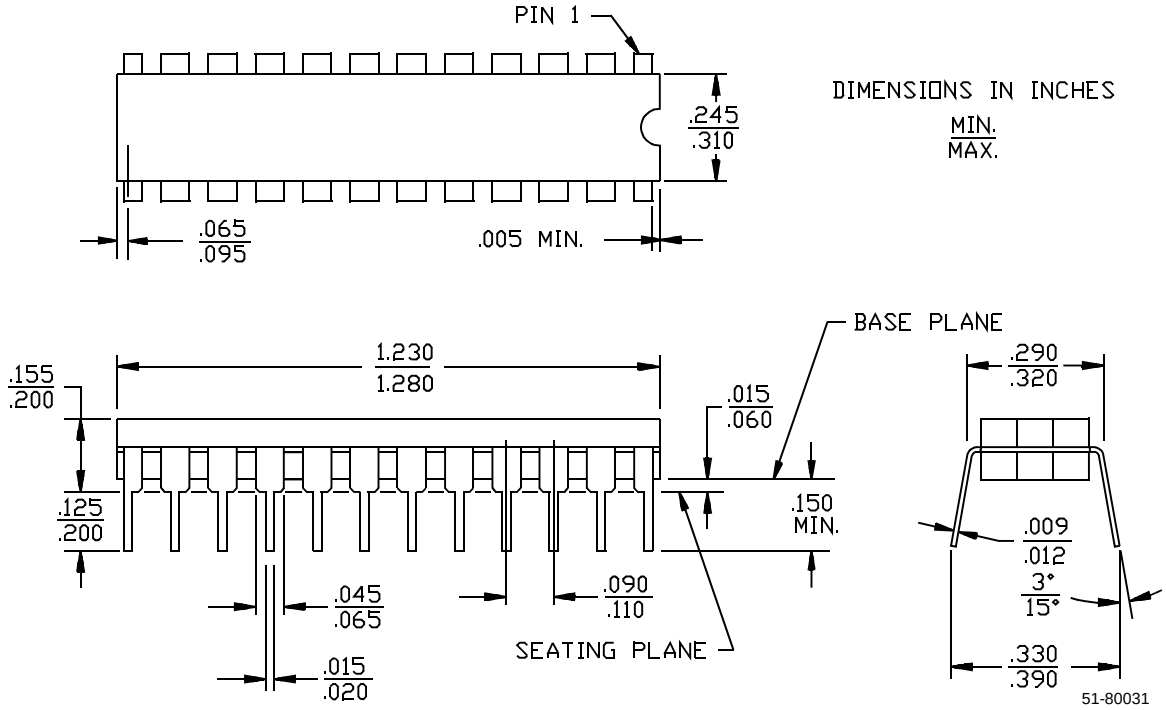
Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

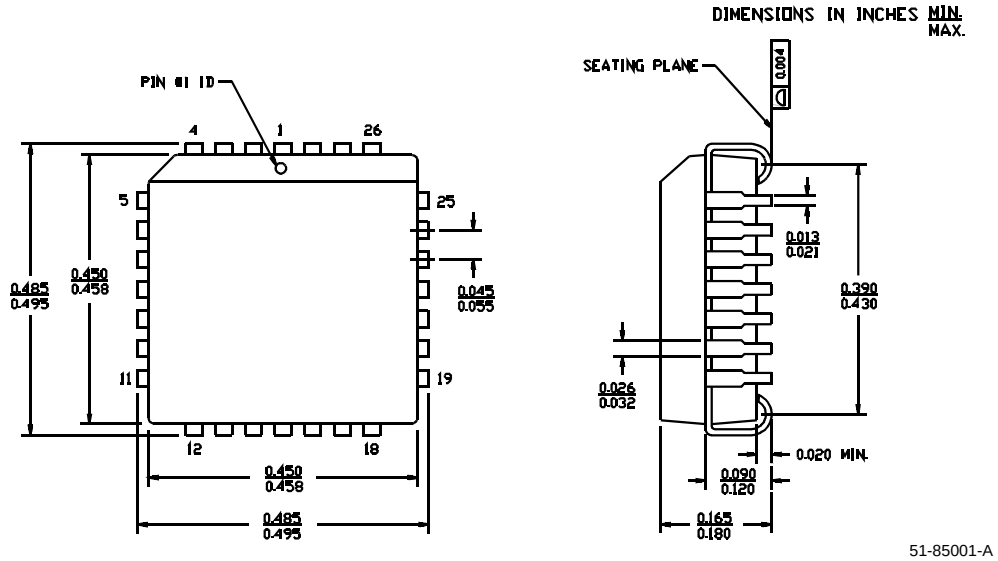
Package Diagrams

24-Lead (300-Mil) CerDIP D14

MIL-STD-1835 D- 9 Config.A



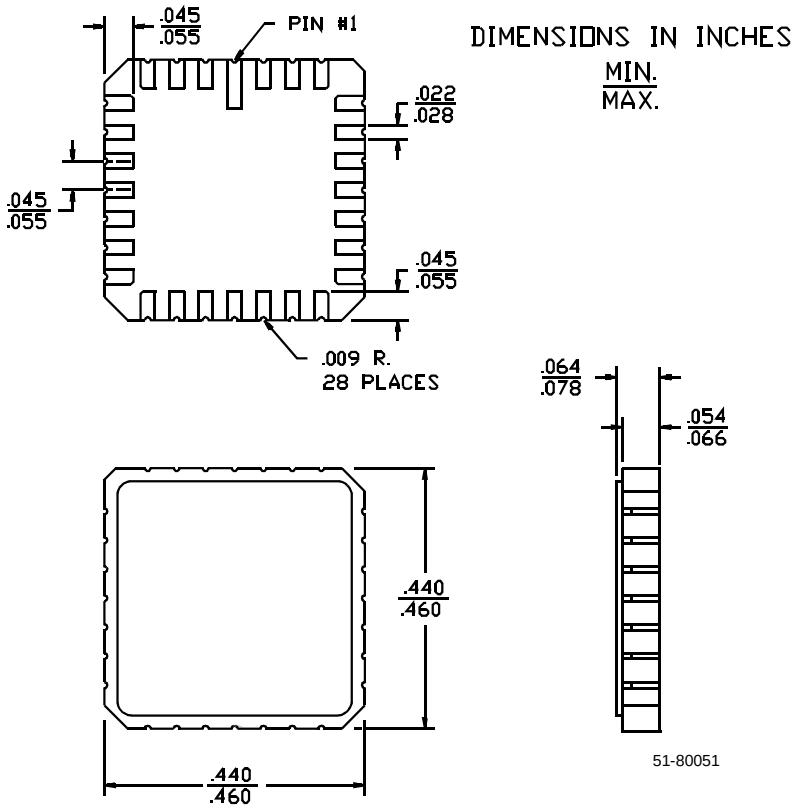
28-Lead Plastic Leaded Chip Carrier J64



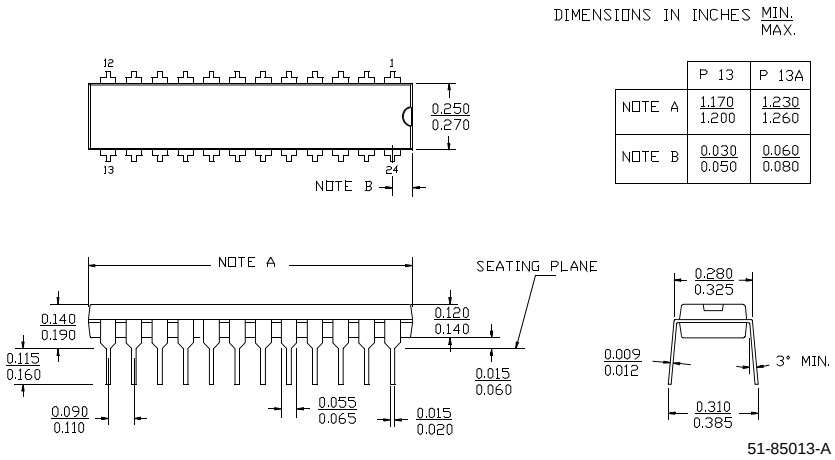
Package Diagrams (continued)

28-Square Leadless Chip Carrier L64

MIL-STD-1835 C-4



24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 / 1.200	1.230 / 1.260
NOTE B	0.030 / 0.050	0.060 / 0.080

Document Title: CY7C235A 1K x 8 Registered PROM Document Number: 38-04002				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113857	03/06/02	DSG	Change from Spec number: 38-00229 to 38-04002

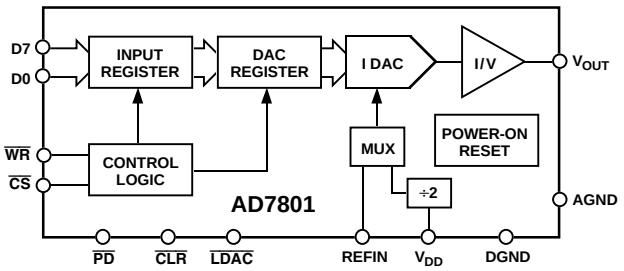
+2.7 V to +5.5 V, Parallel Input, Voltage Output 8-Bit DAC

AD7801

FEATURES
Single 8-Bit DAC
20-Pin SOIC/TSSOP Package
+2.7 V to +5.5 V Operation
Internal and External Reference Capability
DAC Power-Down Function
Parallel Interface
On-Chip Output Buffer Rail-to-Rail Operation
Low Power Operation 1.75 mA max @ 3.3 V
Power-Down to 1 μA max @ 25°C

APPLICATIONS
Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7801 is a single, 8-bit, voltage out DAC that operates from a single +2.7 V to +5.5 V supply. Its on-chip precision output buffer allows the DAC output to swing rail to rail. The AD7801 has a parallel microprocessor and DSP compatible interface with high speed registers and double buffered interface logic. Data is loaded to the input register on the rising edge of $\overline{CS}$ or $\overline{WR}$.

Reference selection for the AD7801 can be either an internal reference derived from the V_{DD} or an external reference applied at the REFIN pin. The output of the DAC can be cleared by using the asynchronous $\overline{CLR}$ input.

The low power consumption of this part makes it ideally suited to portable battery operated equipment. The power consumption is less than 5 mW at 3.3 V, reducing to less than 3 μW in power-down mode.

The AD7801 is available in a 20-lead SOIC and a 20-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Low Power, Single Supply operation. This part operates from a single +2.7 V to +5.5 V supply and consumes typically 5 mW at 3 V, making it ideal for battery powered applications.
2. The on-chip output buffer amplifier allows the output of the DAC to swing rail to rail with a settling time of typically 1.2 μs.
3. Internal or external reference capability.
4. High speed parallel interface.
5. Power-down capability. When powered down the DAC consumes less than 1 μA at 25°C.
6. Packaged in 20-lead SOIC and TSSOP packages.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

AD7801–SPECIFICATIONS

(V_{DD} = +2.7 V to +5.5 V, Internal Reference; C_L = 100 pF, R_L = 10 kΩ to V_{DD} and GND. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Relative Accuracy[2]	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Zero-Code Error @ +25°C	3	LSB typ	All Zeros Loaded to DAC Register
Full-Scale Error	–0.75	LSB typ	All Ones Loaded to DAC Register
Zero-Code Error Drift	100	µV/°C typ	
Gain Error[3]	±1	% FSR typ	
DAC REFERENCE INPUT			
REFIN Input Range	1 to V_{DD}/2	V min/V max	
REFIN Input Impedance	10	MΩ typ	
OUTPUT CHARACTERISTICS			
Output Voltage Range	0 to V_{DD}	V min/V max	
Output Voltage Settling Time	2	µs max	Typically 1.2 µs
Slew Rate	7.5	V/µs typ	
Digital-to-Analog Glitch Impulse	1	nV-s typ	1 LSB Change Around Major Carry
Digital Feedthrough	0.2	nV-s typ	
DC Output Impedance	40	Ω typ	
Short Circuit Current	14	mA typ	
Power Supply Rejection Ratio[4]	0.0003	%/% max	ΔV_{DD} = ±10%
LOGIC INPUTS			
Input Current	±10	µA max	
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = +5 V
V_{INL}, Input Low Voltage	0.6	V max	V_{DD} = +3 V
V_{INH}, Input High Voltage	2.4	V min	V_{DD} = +5 V
V_{INH}, Input High Voltage	2.1	V min	V_{DD} = +3 V
Pin Capacitance	7	pF max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.5	V min/V max	
I_{DD} (Normal Mode)			DAC Active and Excluding Load Current
V_{DD} = 3.3 V			V_{IH} = V_{DD} and V_{IL} = GND
@ 25°C	1.55	mA max	See Figure 6
T_{MIN} to T_{MAX}	1.75	mA max	
V_{DD} = 5.5 V			
@ 25°C	2.35	mA max	
T_{MIN} to T_{MAX}	2.5	mA max	
I_{DD} (Power-Down)			
@ 25°C	1	µA max	V_{IH} = V_{DD} and V_{IL} = GND
T_{MIN} to T_{MAX}	2	µA max	See Figure 18

NOTES
[1]Temperature ranges are as follows: B Version: –40°C to +105°C
[2]Relative Accuracy is calculated using a reduced code range of 15 to 245.
[3]Gain Error is specified between Codes 15 and 245. The actual error at Code 15 is typically 3 LSB.
[4]Guaranteed by characterization at product release, not production tested.

Specifications subject to change without notice.

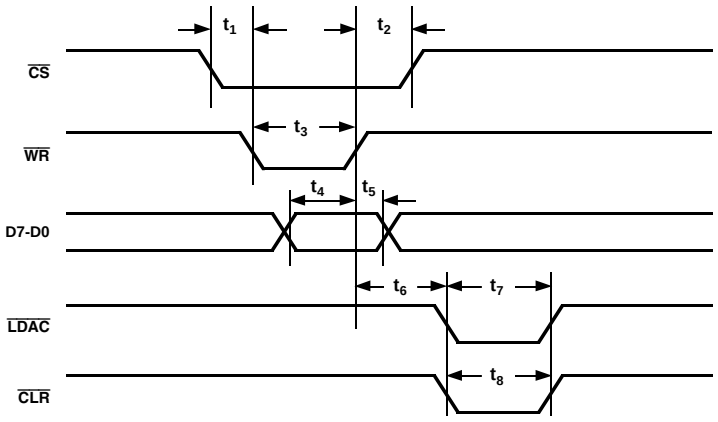


Figure 1. Timing Diagram for Parallel Data Write

TIMING CHARACTERISTICS[1, 2]

(V_{DD} = +2.7 V to +5.5 V; GND = 0 V; Internal V_{DD}/2 Reference. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	0	ns min	Chip Select to Write Setup Time
t_2	0	ns min	Chip Select to Write Hold Time
t_3	20	ns min	Write Pulse Width
t_4	15	ns min	Data Setup Time
t_5	4.5	ns min	Data Hold Time
t_6	20	ns min	Write to $\overline{\text{LDAC}}$ Setup Time
t_7	20	ns min	$\overline{\text{LDAC}}$ Pulse Width
t_8	20	ns min	$\overline{\text{CLR}}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. tr and tf should not exceed 1 µs on any digital input.
[2]See Figure 1.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +7 V
Reference Input Voltage to AGND ....–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND .....–0.3 V to V_{DD} + 0.3 V
AGND to DGND .....–0.3 V to +0.3 V
V_{OUT} to AGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (B Version) ..... –40°C to +105°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature .....+150°C
SSOP Package, Power Dissipation ..... 700 mW
  θ_{JA} Thermal Impedance ..... 143°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) .....+215°C
    Infrared (15 sec) .....+220°C
SOIC Package, Power Dissipation ..... 870 mW
  θ_{JA} Thermal Impedance ..... 74°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) .....+215°C
    Infrared (15 sec) .....+220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

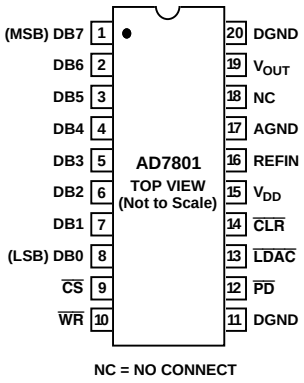
Model	Temperature Range	Package Option*
AD7801BR	–40°C to +105°C	R-20
AD7801BRU	–40°C to +105°C	RU-20

*R = Small Outline; RU = Thin Shrink Small Outline.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7801 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1–8	D7–D0	Parallel Data Inputs. 8-bit data is loaded to the input register of the AD7801 under the control of $\overline{CS}$ and $\overline{WR}$.
9	$\overline{CS}$	Chip Select. Active low logic input.
10	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input used in conjunction with $\overline{CS}$ to write data to the input register.
11	DGND	Digital Ground
12	$\overline{PD}$	Active low input used to put the part into low power mode reducing current consumption to less than 1 μA.
13	$\overline{LDAC}$	Load DAC Logic Input. When this logic input is taken low the DAC output is updated with the contents of its DAC register. If $\overline{LDAC}$ is permanently tied low the DAC is updated on the rising edge of $\overline{WR}$.
14	$\overline{CLR}$	Asynchronous Clear Input (Active Low). When this input is taken low the DAC register is loaded with all zeroes and the DAC output is cleared to zero volts.
15	V_{DD}	Power Supply Input. This part can be operated from +2.7 V to +5.5 V and should be decoupled to GND.
16	REFIN	External Reference Input. This can be used as the reference for the DAC. The range on this reference input is 1 V to $V_{DD}/2$. If REFIN is tied directly to V_{DD} the internal $V_{DD}/2$ reference is selected.
17	AGND	Analog Ground reference point and return point for all analog current on the part.
18	NC	No Connect Pin.
19	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier can swing rail to rail on its output.
20	DGND	Digital Ground reference point and return point for all digital current on the part.

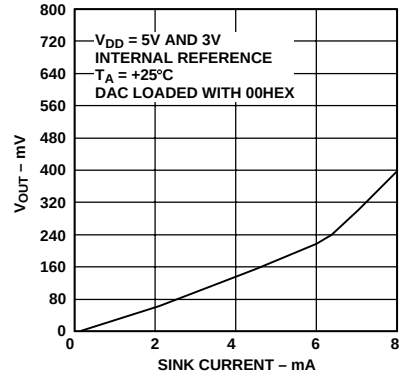


Figure 2. Output Sink Current Capability with V_{DD} = 3 V and V_{DD} = 5 V

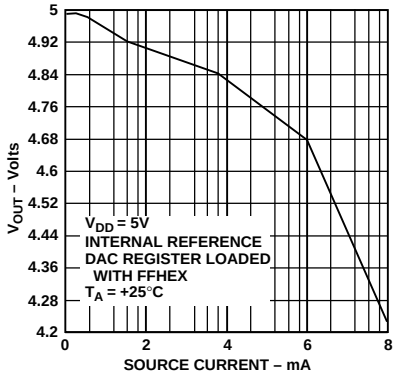


Figure 3. Output Source Current Capability with V_{DD} = 5 V

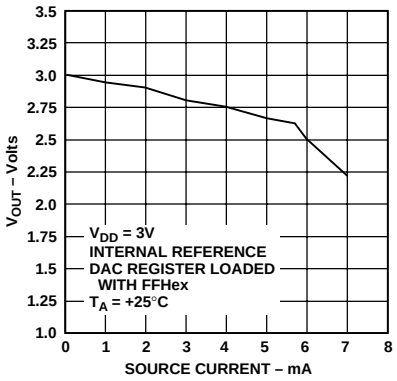


Figure 4. Output Source Current Capability with V_{DD} = 3 V

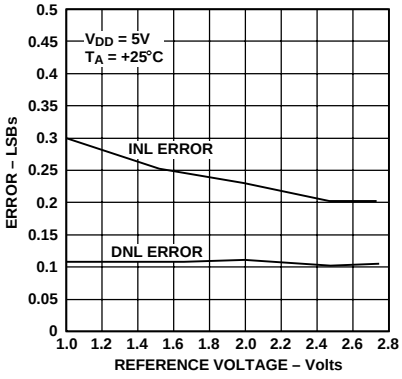


Figure 5. Relative Accuracy vs. External Reference

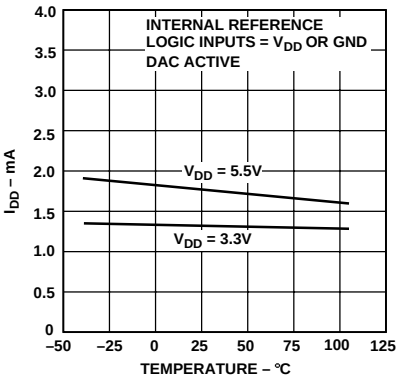


Figure 6. Typical Supply Current vs. Temperature

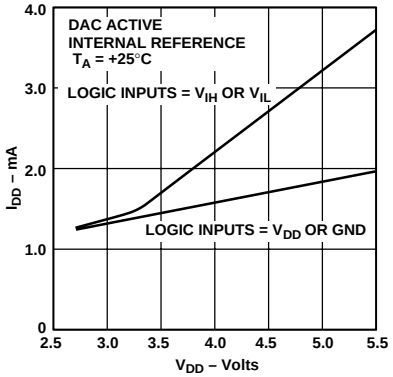


Figure 7. Typical Supply Current vs. Supply Voltage

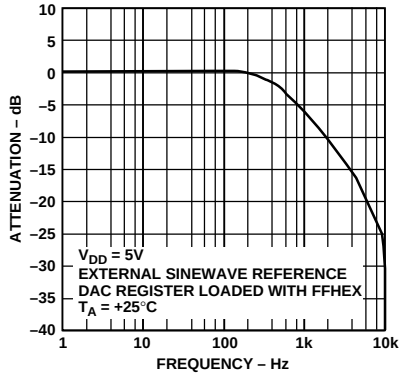


Figure 8. Large Scale Signal Frequency Response

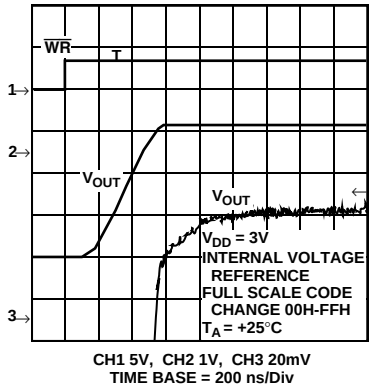


Figure 9. Full-Scale Settling Time

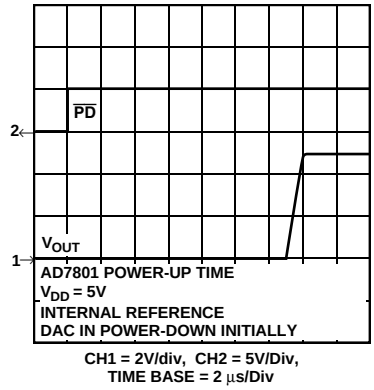


Figure 10. Exiting Power-Down (Full Power-Down)

AD7801–Typical Performance Characteristics

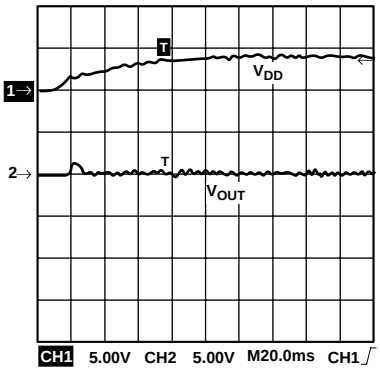


Figure 11. Power-On—Reset

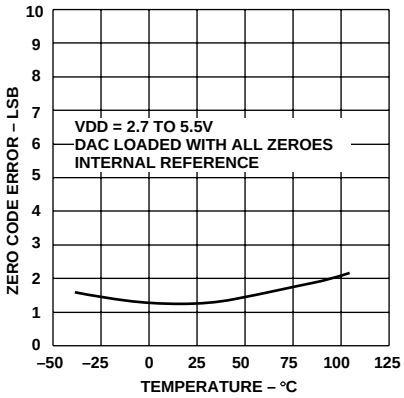


Figure 12. Zero Code Error vs. Temperature

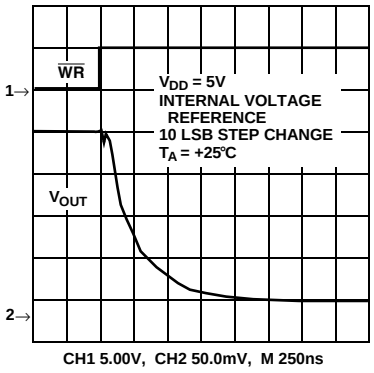


Figure 13. Small-Scale Settling Time

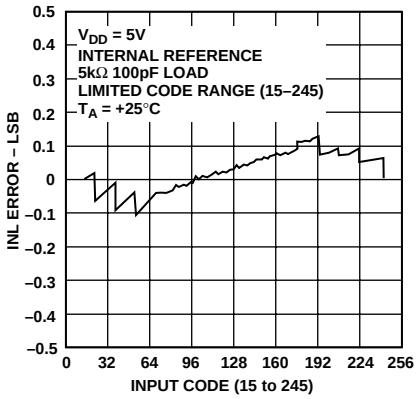


Figure 14. Integral Linearity Plot

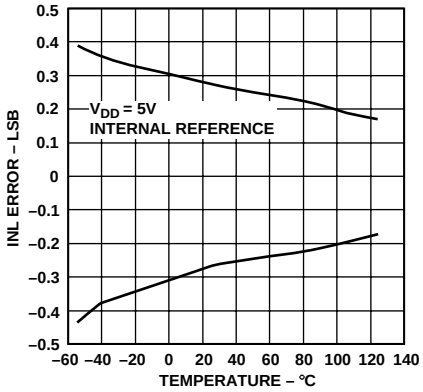


Figure 15. Typical INL vs. Temperature

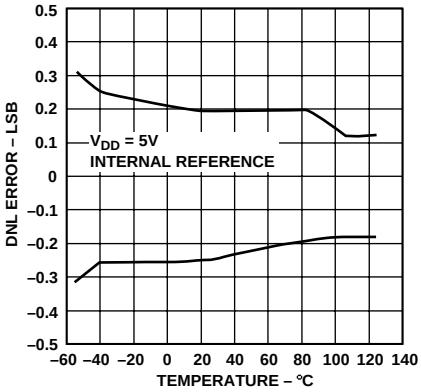


Figure 16. Typical DNL vs. Temperature

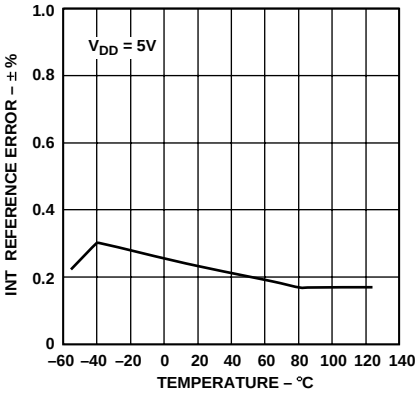


Figure 17. Typical Internal Reference Error vs. Temperature

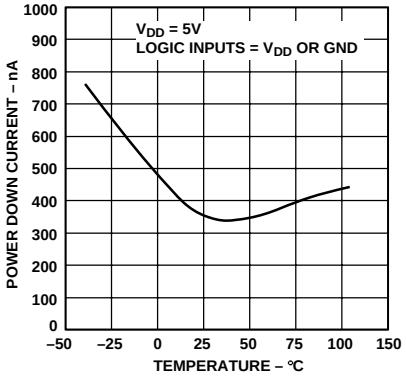


Figure 18. Power-Down Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity

For the DAC, Relative Accuracy or End-Point nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A graphical representation of the transfer curve is shown in Figure 14.

Differential Nonlinearity

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Zero-Code Error

Zero-Code Error is the measured output voltage from V_{OUT} of the DAC when zero code (all zeros) is loaded to the DAC latch. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in LSBs.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale value. It includes full-scale errors but not offset errors.

Digital-to-Analog Glitch Impulse

Digital-to-Analog Glitch Impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected and the $\overline{\text{LDAC}}$ used to update the DAC. It is normally specified as the area of the glitch in nV-secs and measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough

Digital Feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital inputs of the same DAC, but is measured when the DAC is not updated. It is specified in nV-secs and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

Power Supply Rejection Ratio (PSRR)

This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power supply rejection ratio is quoted in terms of % change in output per % change in V_{DD} for full-scale output of the DAC. V_{DD} is varied ±10%.

GENERAL DESCRIPTION

D/A Section

The AD7801 is an 8-bit voltage output digital-to-analog converter. The architecture consists of a reference amplifier and a current source DAC followed by a current-to-voltage converter capable of generating rail-to-rail voltages on the output of the DAC. Figure 19 shows a block diagram of the basic DAC architecture.

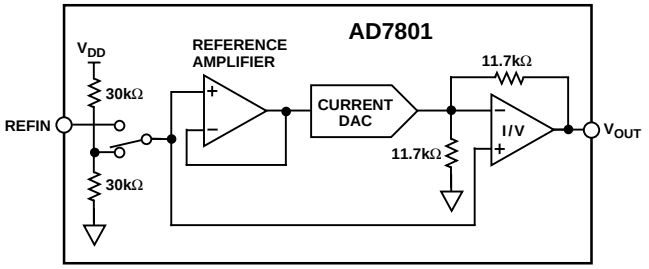


Figure 19. DAC Architecture

The DAC output is internally buffered and has rail-to-rail output characteristics. The output amplifier is capable of driving a load of 100 pF and 10 kΩ to both V_{DD} and ground. The reference selection for the DAC can be either internally generated from V_{DD} or externally applied through the REFIN pin. A comparator on the REFIN pin detects whether the required reference is the internally generated reference or the externally applied voltage to the REFIN pin. If REFIN is connected to V_{DD}, the reference selected is the internally generated $V_{DD}/2$ reference. When an externally applied voltage is more than one volt below V_{DD}, the comparator selection switches to the externally applied voltage on the REFIN pin. The range on the external reference input is from 1.0 V to $V_{DD}/2$ V. The output voltage from the DAC is given by:

$$V_O = 2V_{REF} \times \left(\frac{N}{256}\right)$$

where V_{REF} is the voltage applied to the external REFIN pin or $V_{DD}/2$ when the internal reference is selected. N is the decimal equivalent of the code loaded to the DAC register and ranges from 0 to 255.

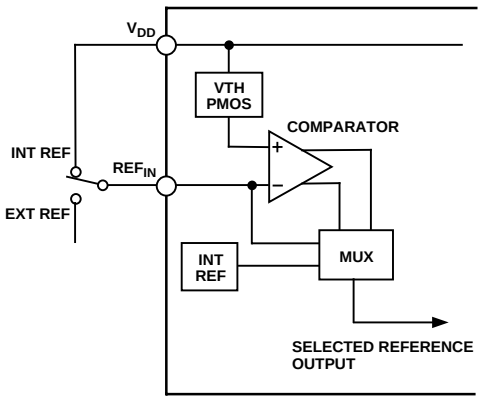


Figure 20. Reference Selection Circuitry

Reference

The AD7801 has the ability to use either an external reference applied through the REFIN pin or an internal reference generated from V_{DD}. Figure 20 shows the reference input arrangement where either the internal $V_{DD}/2$ or the externally applied reference can be selected.

The internal reference is selected by tying the REFIN pin to V_{DD}. If an external reference is to be used, this can be directly applied to the REFIN pin and if this is 1 V below V_{DD}, the internal circuitry will select this externally applied reference as the reference source for the DAC.

Digital Interface

The AD7801 contains a fast parallel interface allowing this DAC to interface to industry standard microprocessors, microcontrollers and DSP machines. There are two modes in which this parallel interface can be configured to update the DAC output. The synchronous update mode allows synchronous updating of the DAC output; the automatic update mode allows the DAC to be updated individually following a write cycle. Figure 21 shows the internal logic associated with the digital interface. The PON STRB signal is internally generated from the power-on reset circuitry and is low during the power-on reset phase of the power up procedure.

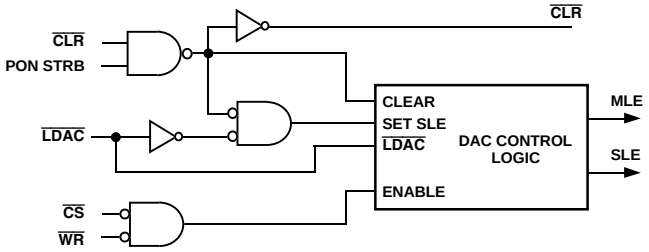


Figure 21. Logic Interface

The AD7801 has a double buffered interface, which allows for synchronous updating of the DAC output. Figure 22 shows a block diagram of the register arrangement within the AD7801.

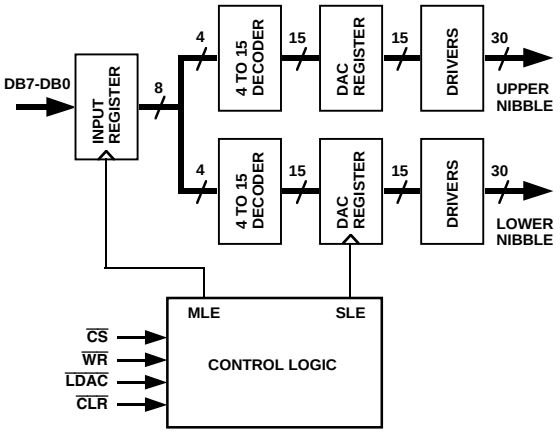


Figure 22. Register Arrangement

Automatic Update Mode

In this mode of operation the $\overline{LDAC}$ signal is permanently tied low. The state of the $\overline{LDAC}$ is sampled on the rising edge of $\overline{WR}$. $\overline{LDAC}$ being low allows the DAC register to be automatically updated on the rising edge of $\overline{WR}$. The output update occurs on the rising edge of $\overline{WR}$. Figure 23 shows the timing associated with the automatic update mode of operation and also the status of the various registers during this frame.

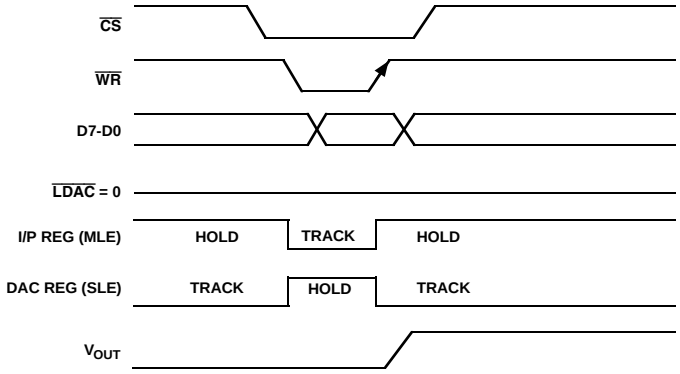


Figure 23. Timing and Register Arrangement for Automatic Update Mode

Synchronous Update Mode

In this mode of operation the $\overline{LDAC}$ signal is used to update the DAC output to synchronize with other updates in the system. The state of the $\overline{LDAC}$ is sampled on the rising edge of $\overline{WR}$. If $\overline{LDAC}$ is high, the automatic update mode is disabled and the DAC latch is updated at any time after the write by taking $\overline{LDAC}$ low. The output update occurs on the falling edge of $\overline{LDAC}$. $\overline{LDAC}$ must be taken back high again before the next data transfer takes place. Figure 24 shows the timing associated with the synchronous update mode of operation and also the status of the various registers during this frame.

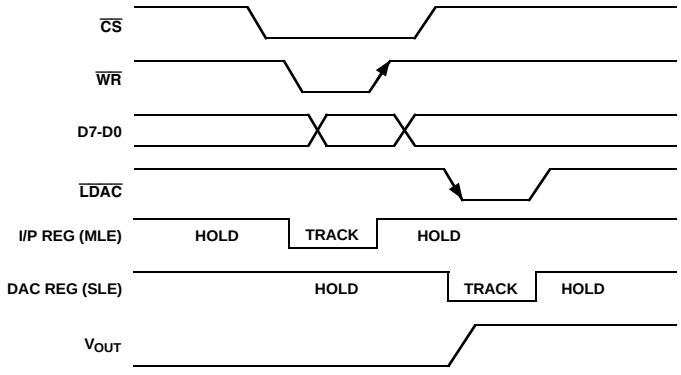


Figure 24. Timing and Register Arrangement for Synchronous Update Mode

POWER-ON RESET

The AD7801 has a power-on reset circuit designed to allow output stability during power up. This circuit holds the DAC in a reset state until a write takes place to the DAC. In the reset state all zeros are latched into the input register of the DAC and the DAC register is in transparent mode thus the output of the DAC is held at ground potential until a write takes place to the DAC. The power-on reset circuitry generates a PON STRB signal which is a gating signal used within the logic to identify a power-on condition.

POWER-DOWN FEATURES

The AD7801 has a power-down feature implemented by exercising the external $\overline{PD}$ pin. An active low signal puts the complete DAC into power-down mode. When in power-down, the current consumption of the device is reduced to less than 1 μA max at +25°C or 2 μA max over temperature, making the device suitable for use in portable battery powered equipment. The internal reference resistors, the reference bias servo loop, the output amplifier and associated linear circuitry are all shut down when the power-down is activated. The output terminal sees a load of ≈ 23 kΩ to GND when in power-down mode as shown in Figure 25. The contents of the data register are unaffected when in power-down mode. The device typically comes out of power-down in 13 μs (see Figure 10).

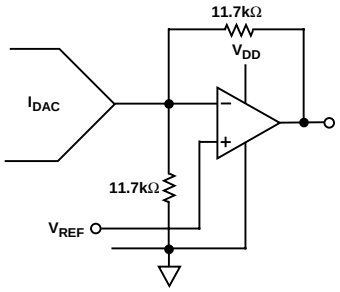


Figure 25. Output Stage During Power-Down

Analog Outputs

The AD7801 contains a voltage output DAC with 8-bit resolution and rail-to-rail operation. The output buffer provides a gain of two at the output. Figures 2, 3 and 4 show the source and sink capabilities of the output amplifier. The slew rate of the output amplifier is typically 7.5 V/μs and has a full-scale settling to eight bits with a 100 pF capacitive load in typically 1.2 μs.

The input coding to the DAC is straight binary. Table I shows the binary transfer function for the AD7801. Figure 26 shows the DAC transfer function for binary coding. Any DAC output voltage can be expressed as:

$$V_{OUT} = 2 \times V_{REF}\left(\frac{N}{256}\right)$$

where:

N is the decimal equivalent of the binary input code. N ranges from 0 to 255.

V_{REF} is the voltage applied to the external REFIN pin when the external reference is selected and is $V_{DD}/2$ if the internal reference is used.

Table I. Output Voltage for Selected Input Codes

Digital MSB . . . LSB	Analog Output
1111 1111	$2 \times \frac{255}{256} \times V_{REF} V$
1111 1110	$2 \times \frac{254}{256} \times V_{REF} V$
1000 0001	$2 \times \frac{129}{256} \times V_{REF} V$
1000 0000	V_{REF} V
0111 1111	$2 \times \frac{127}{256} \times V_{REF} V$
0000 0001	$2 \times \frac{V_{REF}}{256} V$
0000 0000	0 V

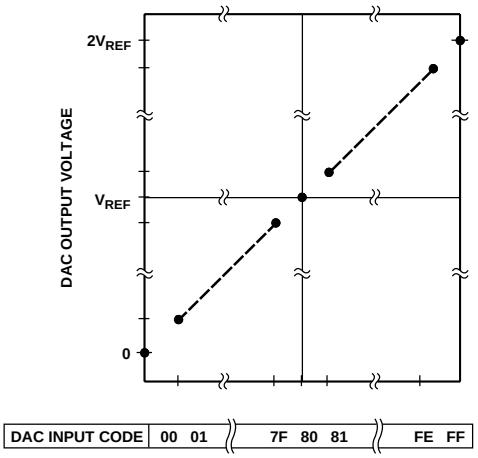


Figure 26. DAC Transfer Function

Figure 27 shows a typical setup for the AD7801 when using its internal reference. The internal reference is selected by tying the REFIN pin to V_{DD}. Internally in the reference section there is a reference detect circuit that will select the internal $V_{DD}/2$ based on the voltage connected to the REFIN pin. If REFIN is within a threshold voltage of a PMOS device (approximately 1 V) of V_{DD} the internal reference is selected. When the REFIN voltage is more than 1 V below V_{DD}, the externally applied voltage at this pin is used as the reference for the DAC. The internal reference on the AD7801 is $V_{DD}/2$, the output current to voltage converter within the AD7801 provides a gain of two. Thus the output range of the DAC is from 0 V to V_{DD}, based on Table I.

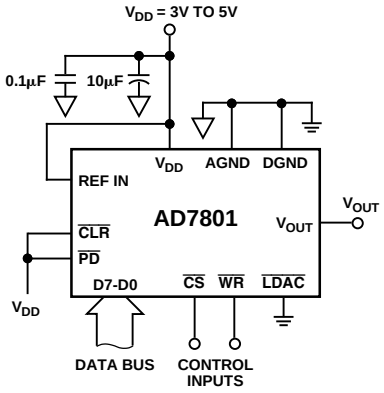


Figure 27. Typical Configuration Selecting the Internal Reference

Figure 28 shows a typical setup for the AD7801 when using an external reference. The reference range for the AD7801 is from 1 V to $V_{DD}/2$ V. Higher values of reference can be incorporated but will saturate the output at both the top and bottom end of the transfer function. There is a gain of two from input to output on the AD7801. Suitable references for 5 V operation are the AD780 and REF192. For 3 V operation a suitable external reference would be the AD589 a 1.23 V bandgap reference.

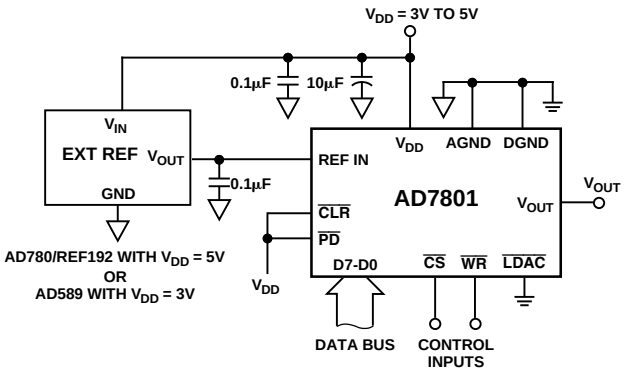


Figure 28. Typical Configuration Using An External Reference

MICROPROCESSOR INTERFACING

AD7801–ADSP-2101/ADSP-2103 Interface

Figure 29 shows an interface between the AD7801 and the ADSP-2101/ADSP-2103. The fast interface timing associated with the AD7801 allows easy interface to the ADSP-2101/ADSP-2103.

$\overline{\text{LDAC}}$ is permanently tied low in this circuit so the DAC output is updated on the rising edge of the $\overline{\text{WR}}$ signal.

Data is loaded to the AD7801 input register using the following ADSP-21xx instruction.

DM(DAC) = MR0

MR0 = ADSP-21xx MR0 Register.
DAC = Decoded DAC Address.

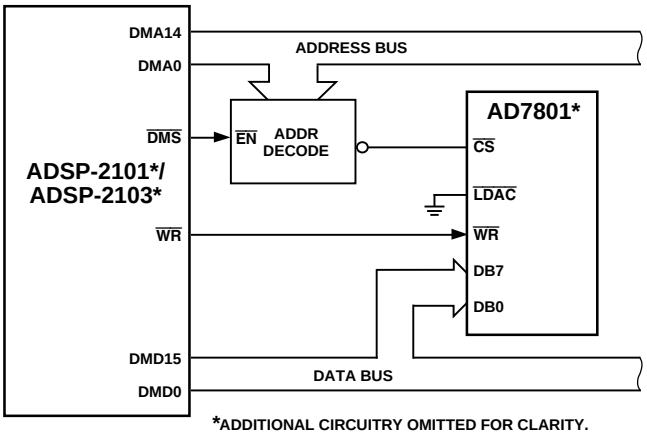


Figure 29. AD7801–ADSP-2101/ADSP-2103 Interface

AD7801–TMS320C20 Interface

Figure 30 shows an interface between the AD7801 and the TMS320C20. Data is loaded to the AD7801 using the following instruction:

OUT DAC, D

DAC = Decoded DAC Address.
D = Data Memory Address.

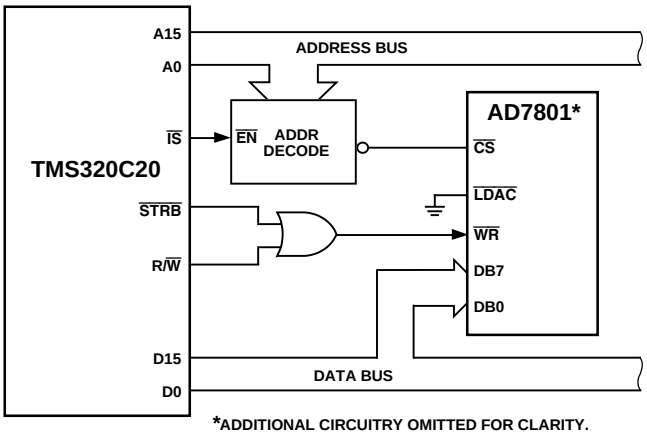


Figure 30. AD7801–TMS320C20 Interface

In the circuit shown the $\overline{LDAC}$ is hardwired low thus the DAC output is updated on the rising edge of $\overline{WR}$. Some applications may require synchronous updating of the DAC in the AD7801. In this case the $\overline{LDAC}$ signal can be driven from an external timer or can be controlled by the microprocessor. One option for synchronous updating is to decode the $\overline{LDAC}$ from the address bus so a write operation at this address will synchronously update the DAC output. A simple OR gate with one input driven from the decoded address and the second input from the $\overline{WR}$ signal will implement this function.

AD7801–8051/8088 Interface

Figure 31 shows a serial interface between the AD7801 and the 8051/8088 processors.

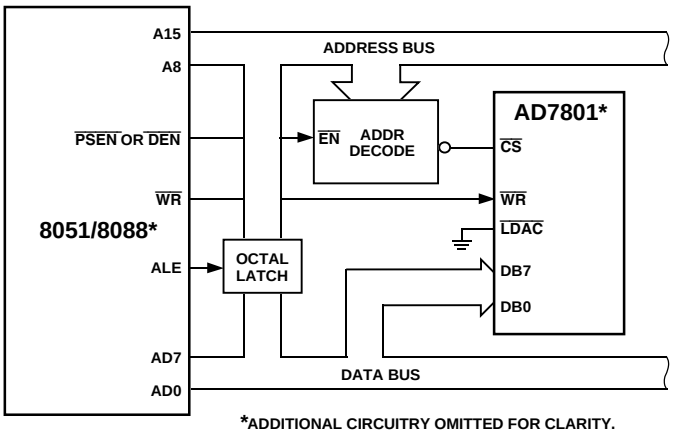


Figure 31. AD7801–8051/8088 Interface

APPLICATIONS

Bipolar Operation Using the AD7801

The AD7801 has been designed for unipolar operation but bipolar operation is possible using the circuit in Figure 32. The circuit shown is configured for an output voltage range of –5 V to +5 V. Rail-to-rail operation at the amplifier output is achievable by using an AD820 or OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[R_2\left(1+\frac{R4}{R3}\right)/\left(R1+R2\right)\times\left(\frac{2V_{REF}D}{256}\right)-V_{REF}\left(\frac{R4}{R3}\right)\right]$$

Where D is the decimal equivalent of the code loaded to the DAC and V_{REF} is the reference voltage input.

With V_{REF} = 2.5 V, R1 = R3 = 10 kΩ and R2 = R4 = 20 kΩ and V_{DD} = 5 V.

$$V_O = \left(\frac{10D}{256}\right)-5$$

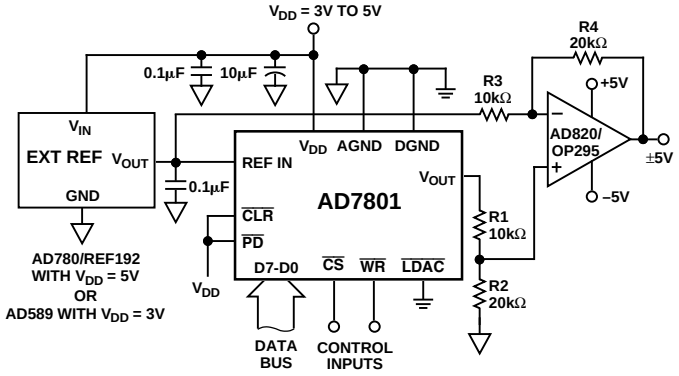


Figure 32. Bipolar Operation Using the AD7801

Decoding Multiple AD7801s in a System

The $\overline{CS}$ pin on the AD7801 can be used in applications to decode a number of DACs. In this application, all DACs in the system receive the same input data, but only the $\overline{CS}$ to one of the DACs will be active at any one time allowing access to one channel in the system. The 74HC139 is used as a two-to-four line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the Enable input on the 74HC139 should be brought to its inactive state while the Coded Address inputs are changing state. Figure 33 shows a diagram of a typical setup for decoding multiple AD7801 devices in a system. The built-in power-on reset circuit on the AD7801 ensures that the outputs of all DACs in the system power up with zero volts on their outputs.

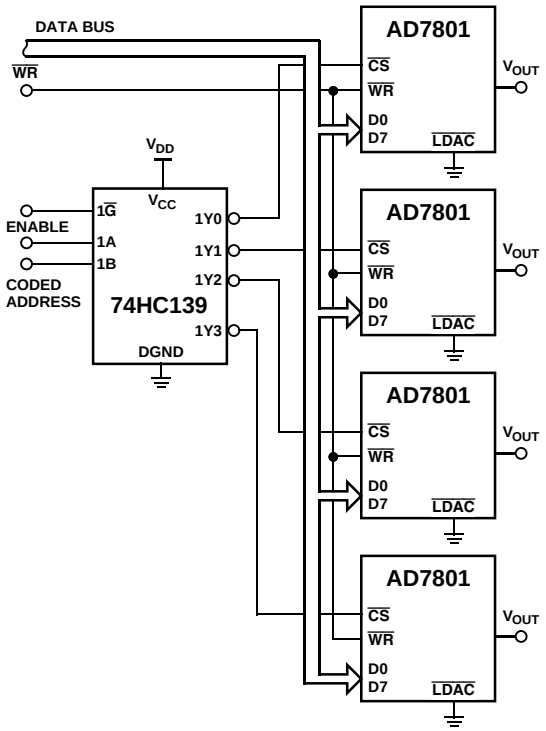


Figure 33. Decoding Multiple AD7801s

AD7801 as a Digitally Programmable Indicator

A digitally programmable upper limit detector using the DAC is shown in Figure 34. The upper limit for the test is loaded to the DAC, which in turn sets the limit for the CMP04. If a signal at the V_{IN} input is not below the programmed value, an LED will indicate the Fail condition.

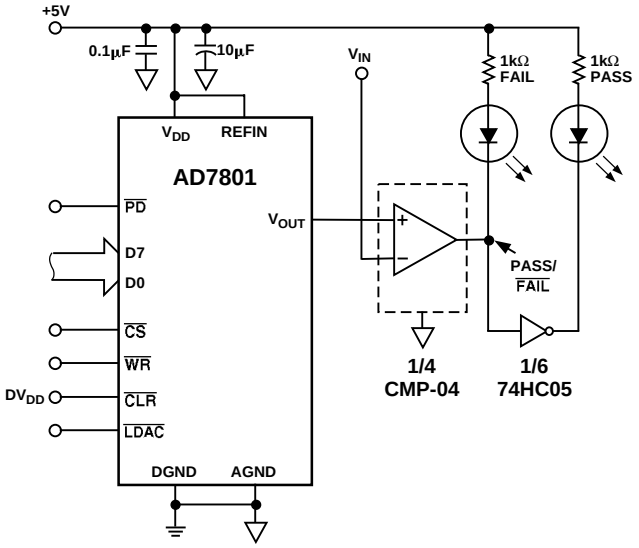


Figure 34. Digitally Programmable Indicator

Programmable Current Source

Figure 35 shows the AD7801 used as the control element of a programmable current source. In this circuit the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the full-scale setting resistor of 470 Ω. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a minimum V_{SOURCE} of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both of which have rail-to-rail operation on their outputs. The current for any digital input code can be calculated as follows:

$$I = \frac{\left(2\,V_{REF}\,D\right)}{\left(256\ (5\ k\Omega)\right)}$$

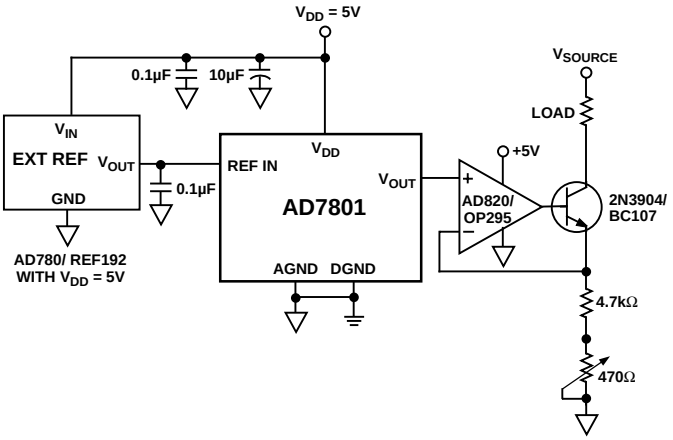


Figure 35. Programmable Current Source

Coarse and Fine Adjustment using two AD7801s

The two DACs can be paired together to form a coarse and fine adjustment function for a setpoint as shown in Figure 36. In this circuit, the first DAC is used to provide the coarse adjustment and the second DAC is used to provide the fine adjustment. Varying the ratio of R1 and R2 will vary the relative effect of the coarse and fine tune elements in the circuit. For the resistor values shown, the second DAC has a resolution of 148 µV giving a fine tune range of 38 mV (approximately 2 LSB) for operation with a V_{DD} of 5 V and a reference of 2.5 V. The amplifier shown allows a rail-to-rail output voltage to be achieved on the output. A typical application for the circuit would be in a setpoint controller.

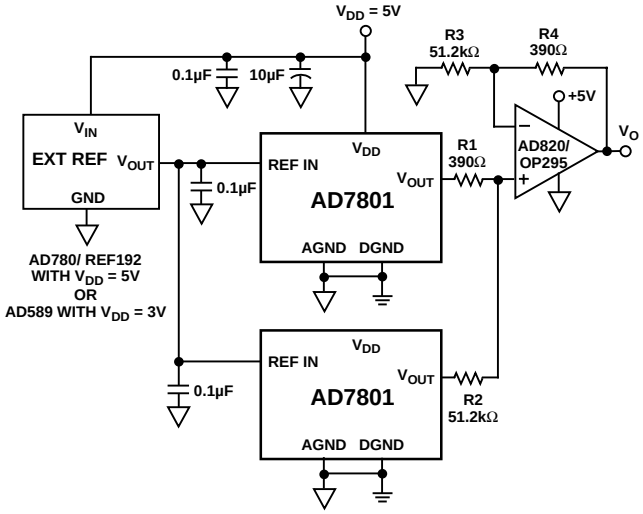


Figure 36. Coarse and Fine Adjustment

Power Supply Bypassing and Grounding

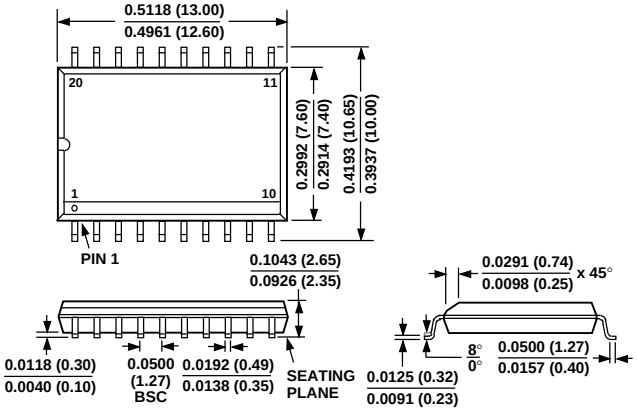
In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD7801 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD7801 is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only, a star ground point which should be established as closely as possible to the AD7801. The AD7801 should have ample supply bypassing of 10 µF in parallel with 0.1 µF located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitors should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD7801 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effect of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

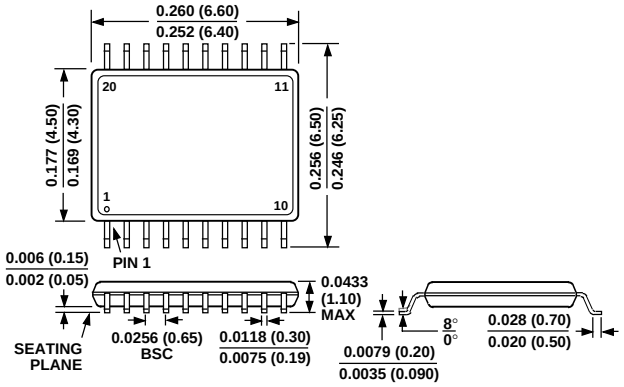
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Wide Body SOIC
(R-20)



20-Lead TSSOP
(RU-20)



C2995–12–4/97

PRINTED IN U.S.A.

ANALOG DEVICES

Very Low Noise Quad Operational Amplifier

OP-470

FEATURES

- **Very Low Noise** ..... **5nV/$\sqrt{Hz}$ @ 1kHz Max**
- **Excellent Input Offset Voltage** ..... **0.4mV Max**
- **Low Offset Voltage Drift** ..... **2μV/°C Max**
- **Very High Gain** ..... **1000V/mV Min**
- **Outstanding CMR** ..... **110dB Min**
- **Slew Rate** ..... **2V/μs Typ**
- **Gain-Bandwidth Product** ..... **6MHz Typ**
- **Industry Standard Quad Pinouts**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	LCC*	
400	–	–	OP470ARC/883	MIL
400	OP470AY*	–	OP470ATC/883	MIL
400	OP470EY	–	–	IND
800	OP470FY	–	–	IND
1000	–	OP470GP	–	XIND
1000	–	OP470GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

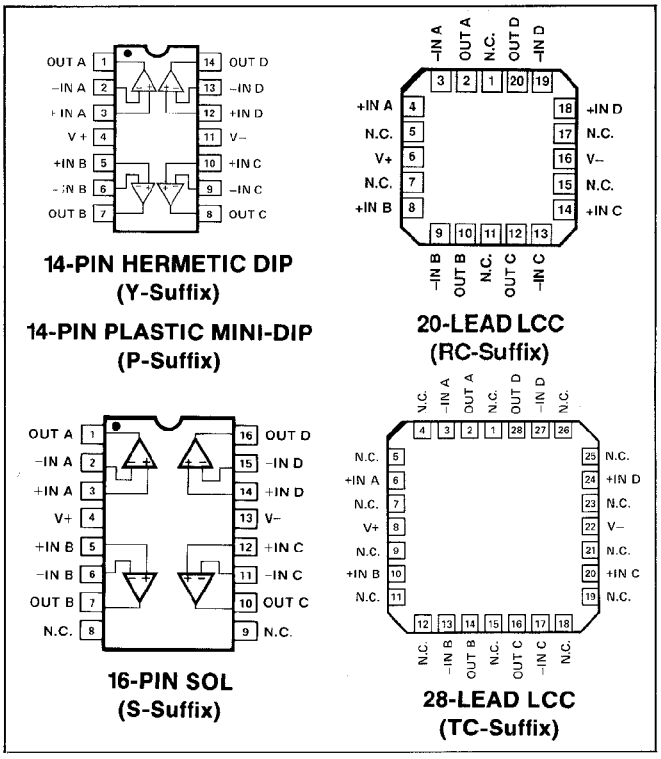
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-470 is a high-performance monolithic quad operational amplifier with exceptionally low voltage noise, 5nV/$\sqrt{Hz}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

The OP-470 features an input offset voltage below 0.4mV, excellent for a quad op amp, and an offset drift under 2μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP-470 is over 1,000,000 into a 10kΩ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 25nA which reduces errors due to signal source resistance. The OP-470's CMR of over 110dB and PSRR of less than 1.8μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP-470 is half that of four OP-27s, a significant advantage for power con-

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)

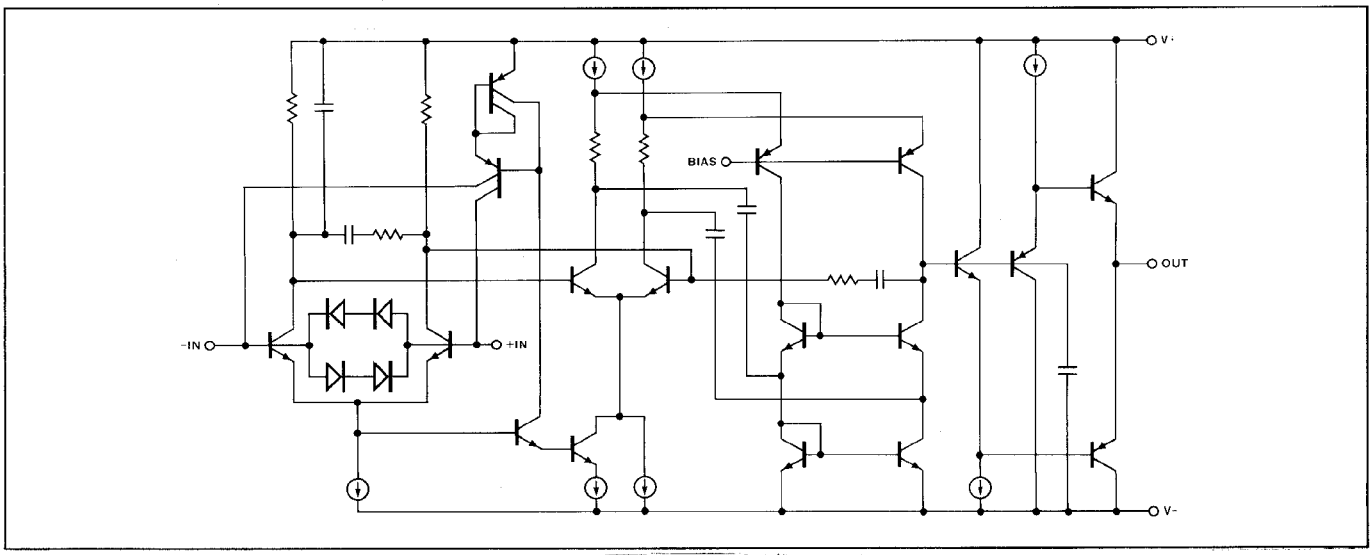
14-PIN PLASTIC MINI-DIP (P-Suffix)

20-LEAD LCC (RC-Suffix)

16-PIN SOL (S-Suffix)

28-LEAD LCC (TC-Suffix)

SIMPLIFIED SCHEMATIC



scious applications. The OP-470 is unity-gain stable with a gain-bandwidth product of 6MHz and a slew rate of 2V/μs.

The OP-470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers, and low-noise active filters.

The OP-470 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-471, with a slew rate of 8V/μs, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C
Operating Temperature Range
OP-470A ..... –55°C to +125°C
OP-470E, OP-470F ..... –25°C to +85°C
OP-470G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-470A/E			OP-470F			OP-470G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.1	0.4	—	0.2	0.8	—	0.4	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	3	10	—	6	20	—	12	30	nA
Input Bias Current	I_B	V_{CM} = 0V	—	6	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	80	200	—	80	200	—	80	200	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	3.8	6.5	—	3.8	6.5	—	3.8	6.5	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	3.3	5.5	—	3.3	5.5	—	3.3	5.5	
		f_O = 1kHz (Note 2)	—	3.2	5.0	—	3.2	5.0	—	3.2	5.0	
Input Noise Current Density	i_n	f_O = 10Hz	—	1.7	—	—	1.7	—	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f_O = 1kHz	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V										V/mV
		R_L = 10kΩ	1000	2300	—	800	1700	—	800	1700	—	
		R_L = 2kΩ	500	1200	—	400	900	—	400	900	—	
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	110	125	—	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	0.56	1.8	—	1.0	5.6	—	1.0	5.6	μV/V
Slew Rate	SR		1.4	2	—	1.4	2	—	1.4	2	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-470A/E MIN	OP-470A/E TYP	OP-470A/E MAX	OP-470F MIN	OP-470F TYP	OP-470F MAX	OP-470G MIN	OP-470G TYP	OP-470G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9	11	—	9	11	—	9	11	mA
Gain Bandwidth Product	GBW	$A_V = +10$	—	6	—	—	6	—	—	6	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	155	—	125	155	—	125	155	—	dB
Input Capacitance	C_{IN}		—	2	—	—	2	—	—	2	—	pF
Input Resistance Differential-Mode	R_{IN}		—	0.4	—	—	0.4	—	—	0.4	—	MΩ
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
Settling Time	t_s	$A_V = +1$ to 0.1% to 0.01%	— —	5.5 6.0	— —	— —	5.5 6.0	— —	— —	5.5 6.0	— —	μs

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$ for OP-470A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470A MIN	OP-470A TYP	OP-470A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.14	0.6	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	15	50	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	750 400	1600 800	— —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	1.0	5.6	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	mA

NOTE:
1. Guaranteed by CMR test.

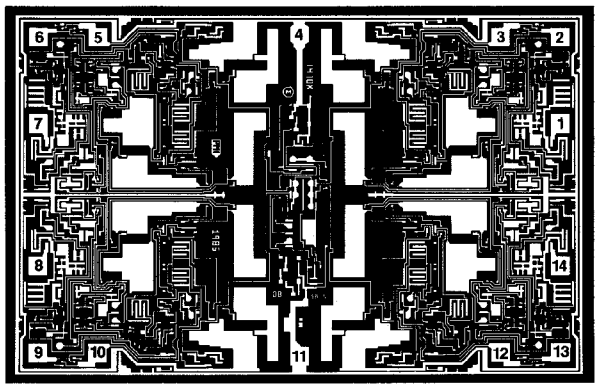
OP-470

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-470E/F, $-40°C \le T_A \le +85°C$ for OP-470G, unless otherwise noted.

			OP-470E			OP-470F			OP-470G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.12	0.5	—	0.24	1.0	—	0.5	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	—	0.6	4	—	2	—	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	4	20	—	7	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	11	50	—	20	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$										
		$R_L = 10k\Omega$	800	1800	—	600	1400	—	600	1500	—	V/mV
		$R_L = 2k\Omega$	400	900	—	300	700	—	300	800	—	
Input Voltage Range	IVR	(Note 1)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	90	115	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	V_S – ±4.5V to ⊥18V	—	0.7	5.6	—	1.8	10	—	1.8	10	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.3	11	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



1. OUT A
2. −IN A
3. +IN A
4. V+
5. +IN B
6. −IN B
7. OUT B
8. OUT C
9. −IN C
10. +IN C
11. V−
12. +IN D
13. −IN D
14. OUT D

DIE SIZE 0.163 × 0.106 inch, 17,278 sq. mils
(4.14 × 2.69 mm, 11.14 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.8	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 800 400	 V/mV MIN
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	5.6	μV/V MAX
Slew Rate	SR		1.4	V/μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	11	mA MAX

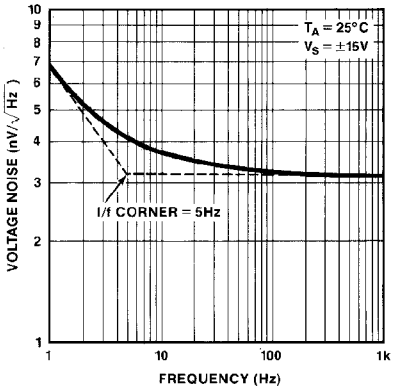
NOTE:
1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

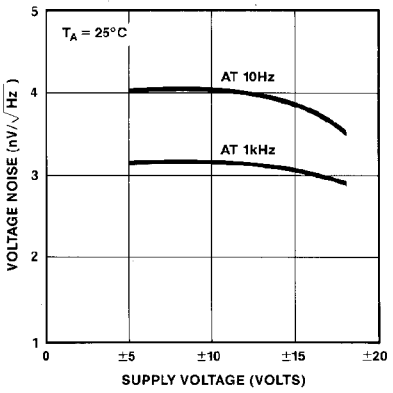
OP-470

TYPICAL PERFORMANCE CHARACTERISTICS

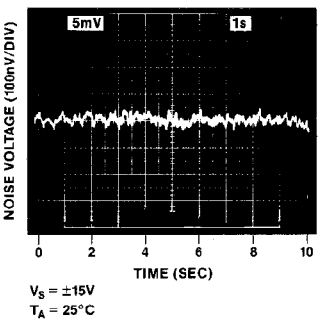
VOLTAGE NOISE DENSITY vs FREQUENCY



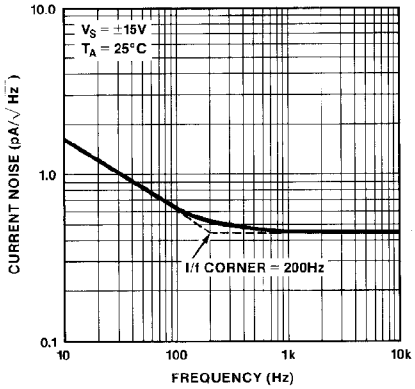
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



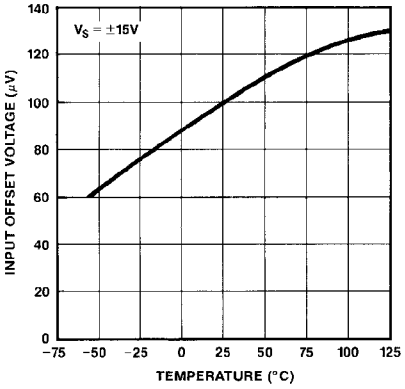
0.1Hz TO 10Hz NOISE



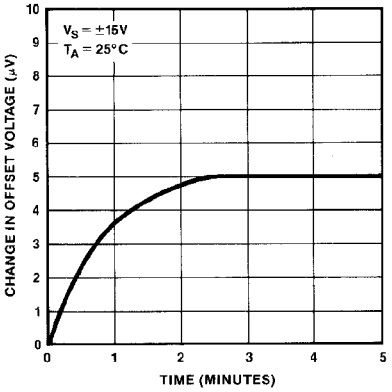
CURRENT NOISE DENSITY vs FREQUENCY



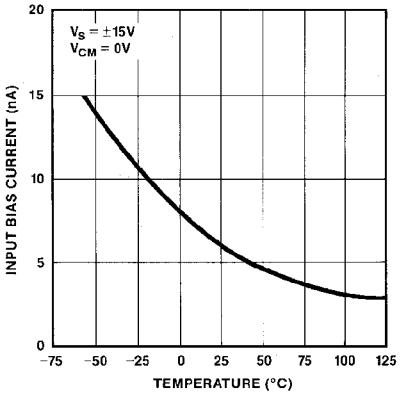
INPUT OFFSET VOLTAGE vs TEMPERATURE



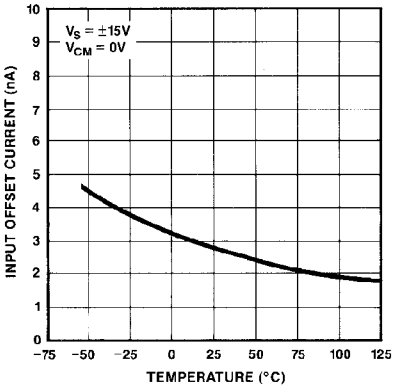
WARM-UP OFFSET VOLTAGE DRIFT



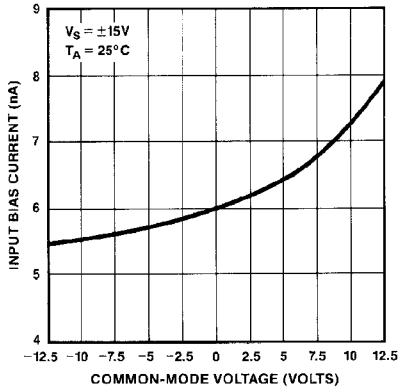
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

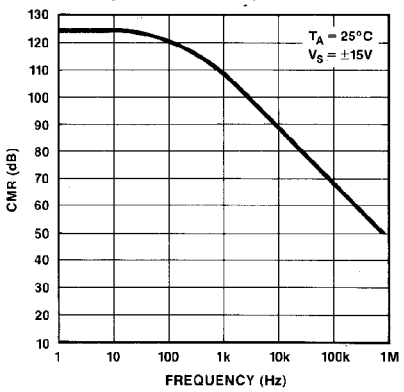


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

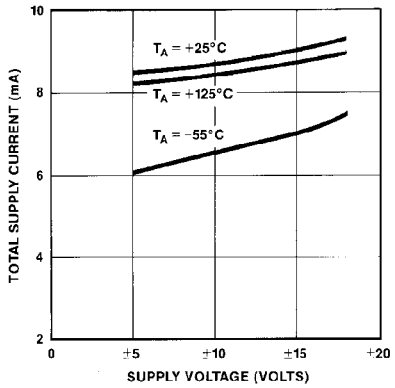


TYPICAL PERFORMANCE CHARACTERISTICS

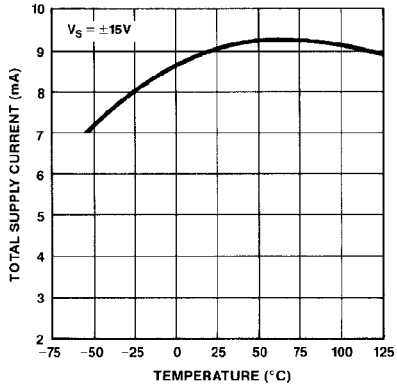
CMR vs FREQUENCY



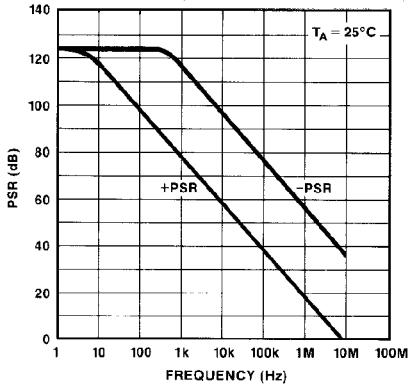
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



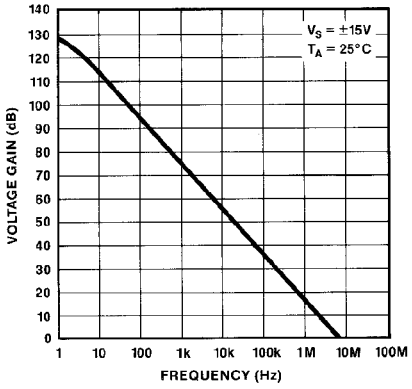
TOTAL SUPPLY CURRENT vs TEMPERATURE



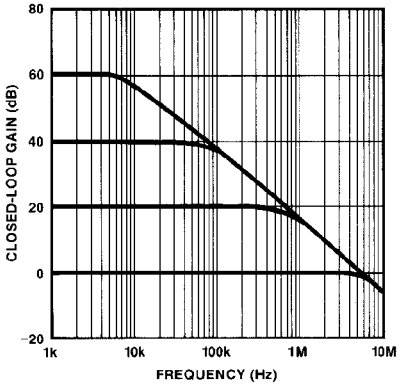
PSR vs FREQUENCY



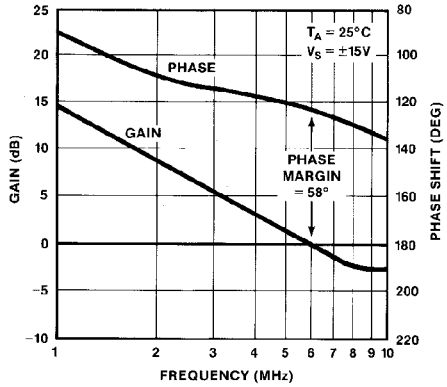
OPEN-LOOP GAIN vs FREQUENCY



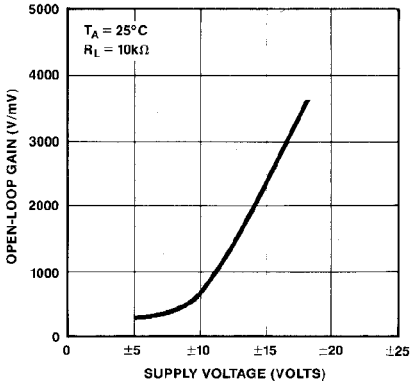
CLOSED-LOOP GAIN vs FREQUENCY



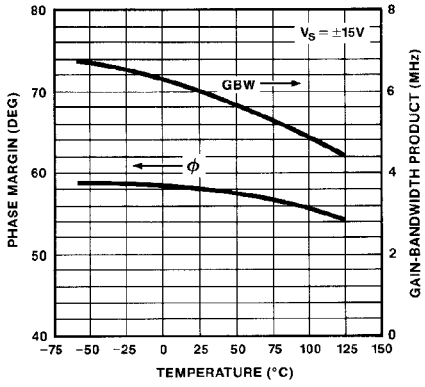
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



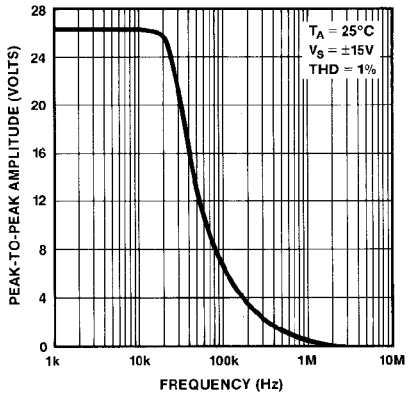
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



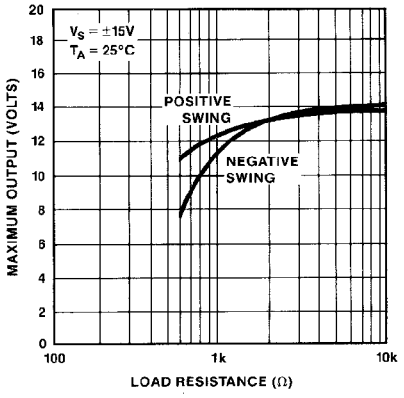
OP-470

TYPICAL PERFORMANCE CHARACTERISTICS

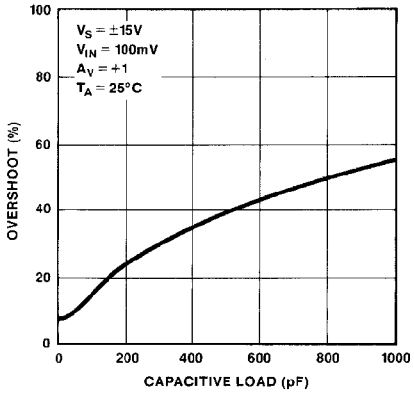
MAXIMUM OUTPUT SWING vs FREQUENCY



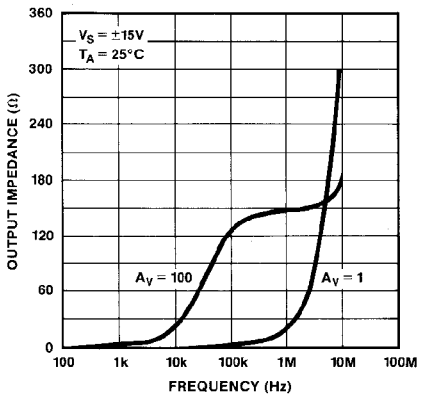
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



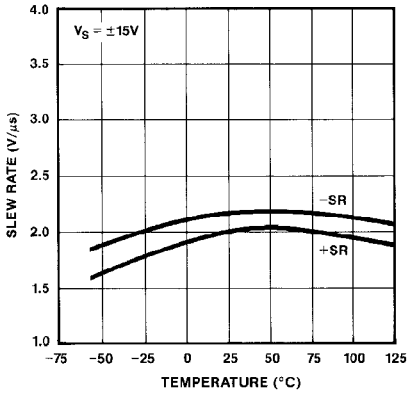
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



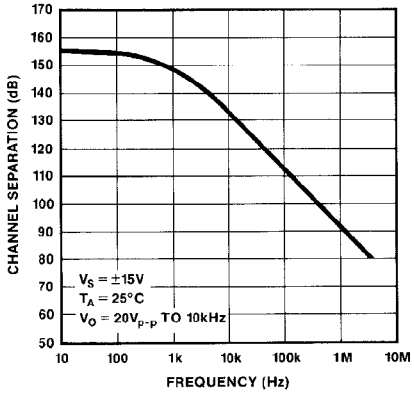
OUTPUT IMPEDANCE vs FREQUENCY



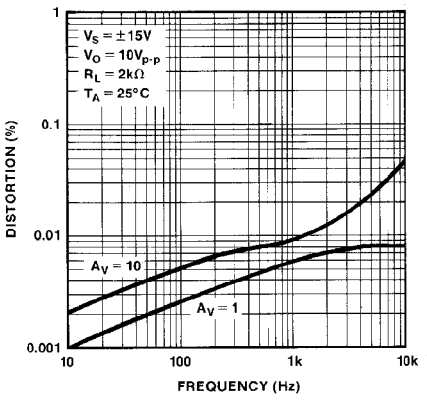
SLEW RATE vs TEMPERATURE



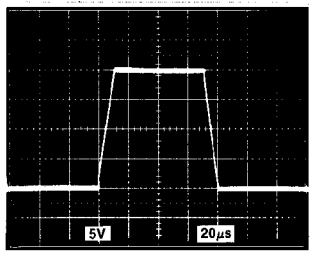
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

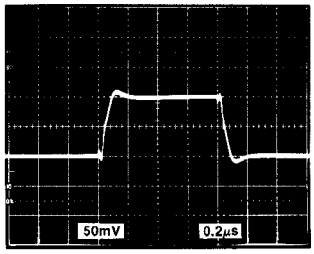


LARGE-SIGNAL TRANSIENT RESPONSE



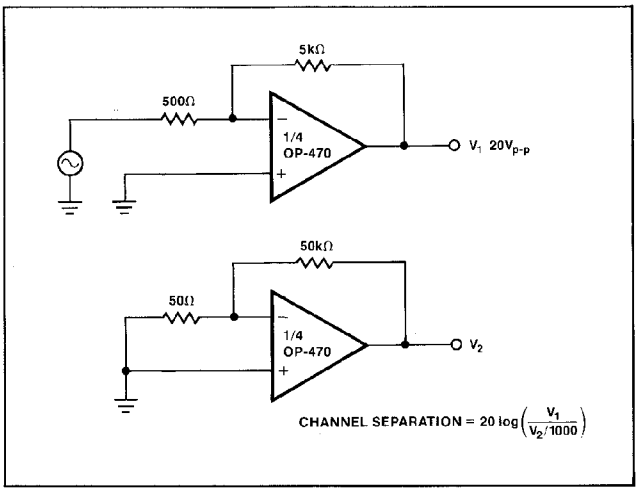
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE

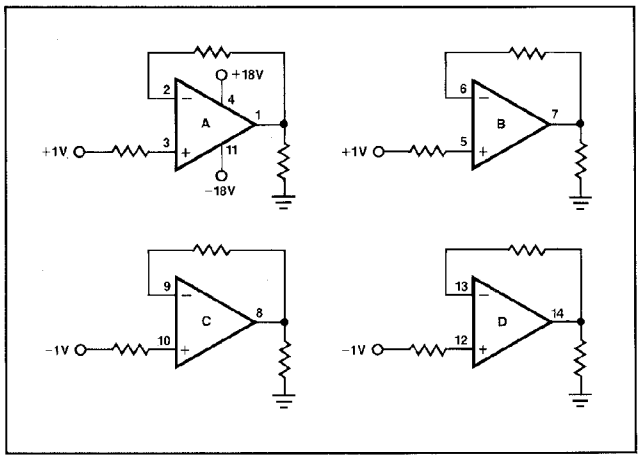


T_A = 25°C
V_S = ±15V
A_V = +1

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-470 is a very low-noise quad op amp, exhibiting a typical voltage noise of only 3.2nV/$\sqrt{Hz}$ @ 1kHz. The exceptionally low noise characteristics of the OP-470 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-470 is gained at the expense of current noise performance, which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calulated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is dominated by the voltage noise of the OP-470. As R_S rises above

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

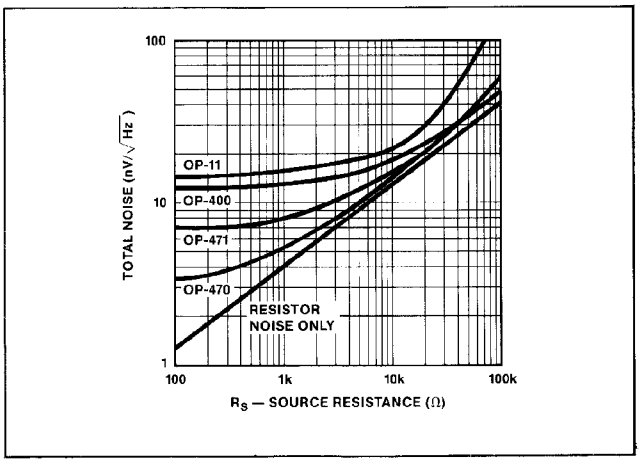
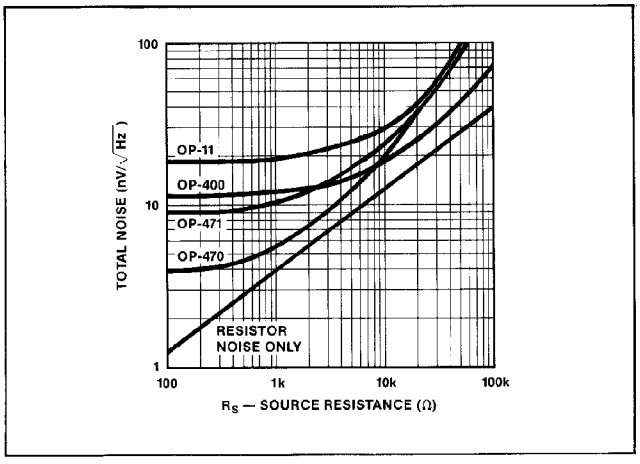


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



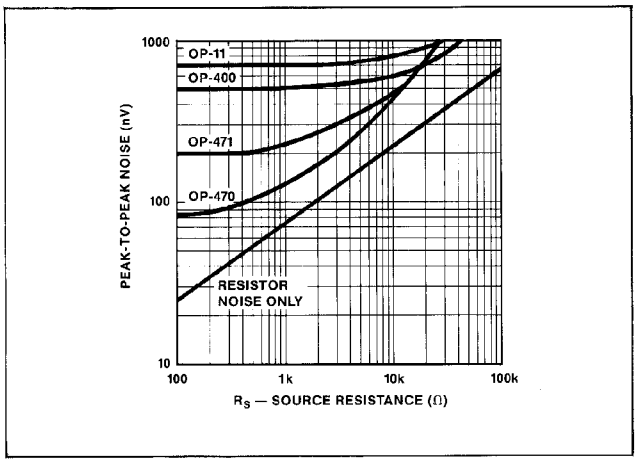
1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-470. When R_S exceeds 20kΩ, current noise of the OP-470 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-470 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-470, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-470 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases. The crossover point between the OP-470 and the OP-400 for peak-to-peak noise is at $R_S = 17k\Omega$.

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)



The OP-471 is a higher speed version of the OP-470, with a slew rate of 8V/μs. Noise of the OP-471 is only slightly higher than the OP-470. Like the OP-470, the OP-471 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table I.

TABLE I

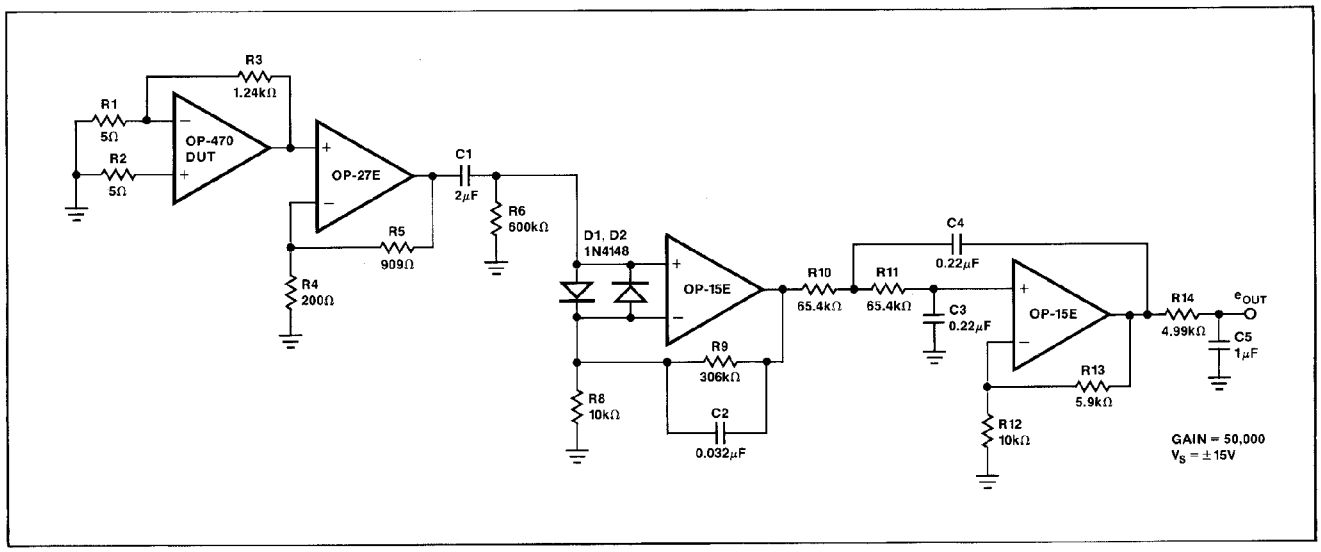
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-470 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-470 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications," Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak

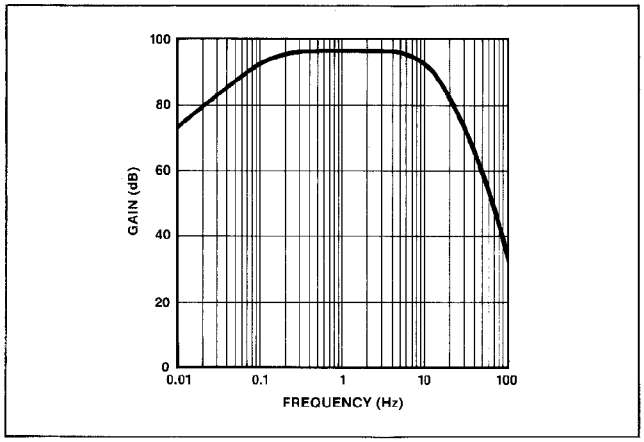
FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



noise specification of the OP-470 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 5μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\left(\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2}\right)$$

The OP-470 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\left(\sqrt{4e_n^2}\right) = 101\ (2e_n)$$

FIGURE 6: Noise Voltage Density Test Circuit

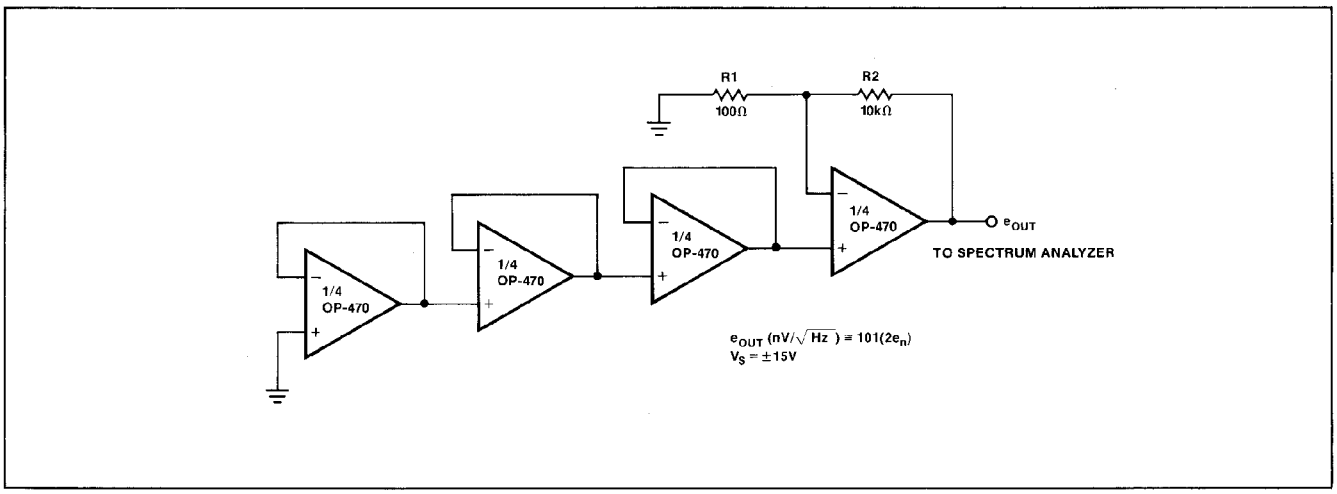
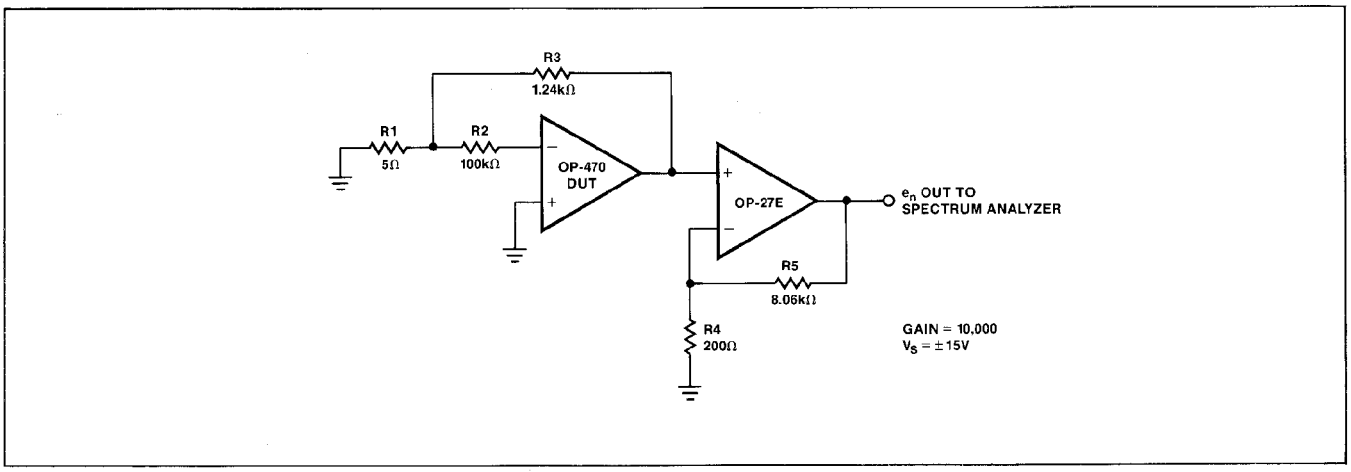


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-470 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-470.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-470.

In applications where the OP-470's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V−, or when V− is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

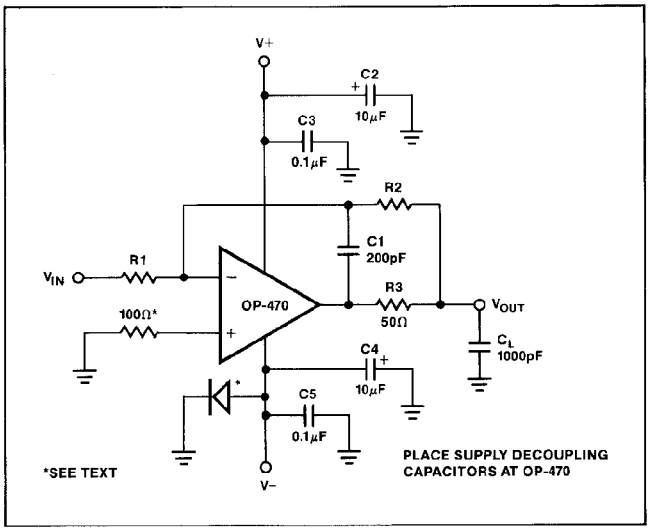
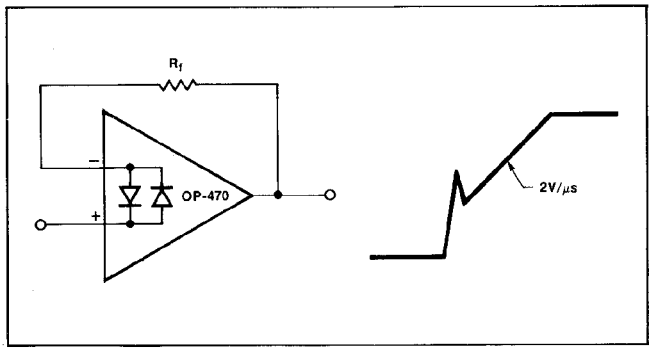


FIGURE 9: Pulsed Operation



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V– is disconnected. It should be noted that any source resistance, even 100Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V– pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (2pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f helps eliminate this problem.

APPLICATIONS

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around $2nV/\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 1000. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω. The amplifier is stable with a 10nF capacitive load and can supply up to 30mA of output drive.

DIGITAL PANNING CONTROL

Figure 12 uses a DAC-8408, a quad 8-bit DAC, to pan a signal between two channels. The complementary DAC current outputs of two of the DAC-8408's four DACs drive current-to-voltage converters built from a single quad OP-470. The amplifiers have complementary outputs with the amplitudes dependent upon the digital code applied to the DAC. Figure 13 shows the complementary outputs for a 1kHz input signal and digital ramp applied to the DAC data inputs. Distortion of the digital panning control is less than 0.01%.

Gain error due to the mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC. Of the four DACs available in the DAC-8408, only two, DACs A and C, actually pass a signal. DACs B and D are used to provide the additional feedback resistors needed in the circuit. If the $V_{REF}B$ and $V_{REF}D$ inputs remain unconnected the currrent-to-voltage converters using $R_{FB}B$ and $R_{FB}D$ are unaffected by digital data reaching DACs B and D.

FIGURE 10: Low Noise Amplifier

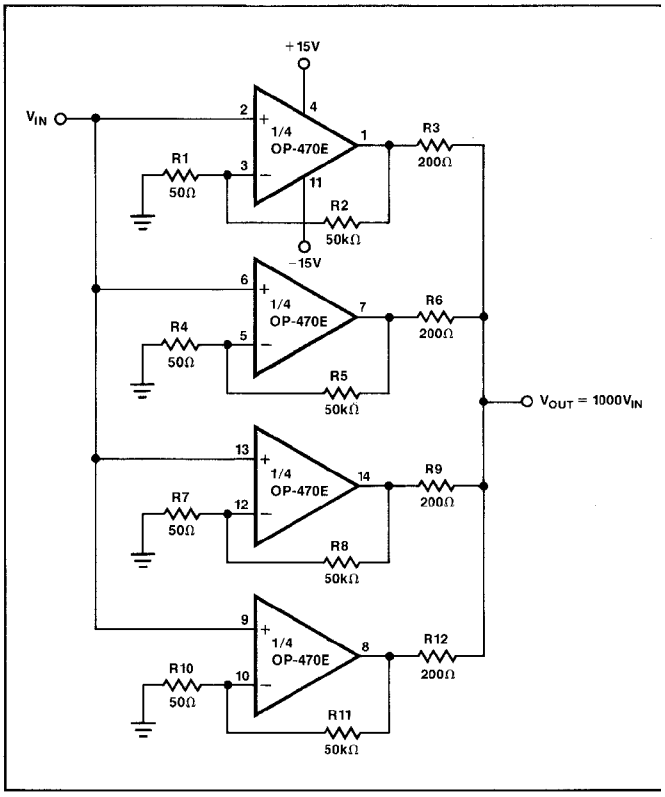


FIGURE 11: Noise Density of Low Noise Amplifier, G = 1000

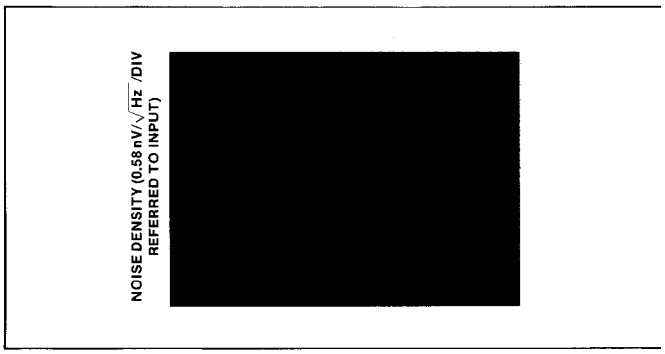


FIGURE 12: Digital Panning Control Circuit

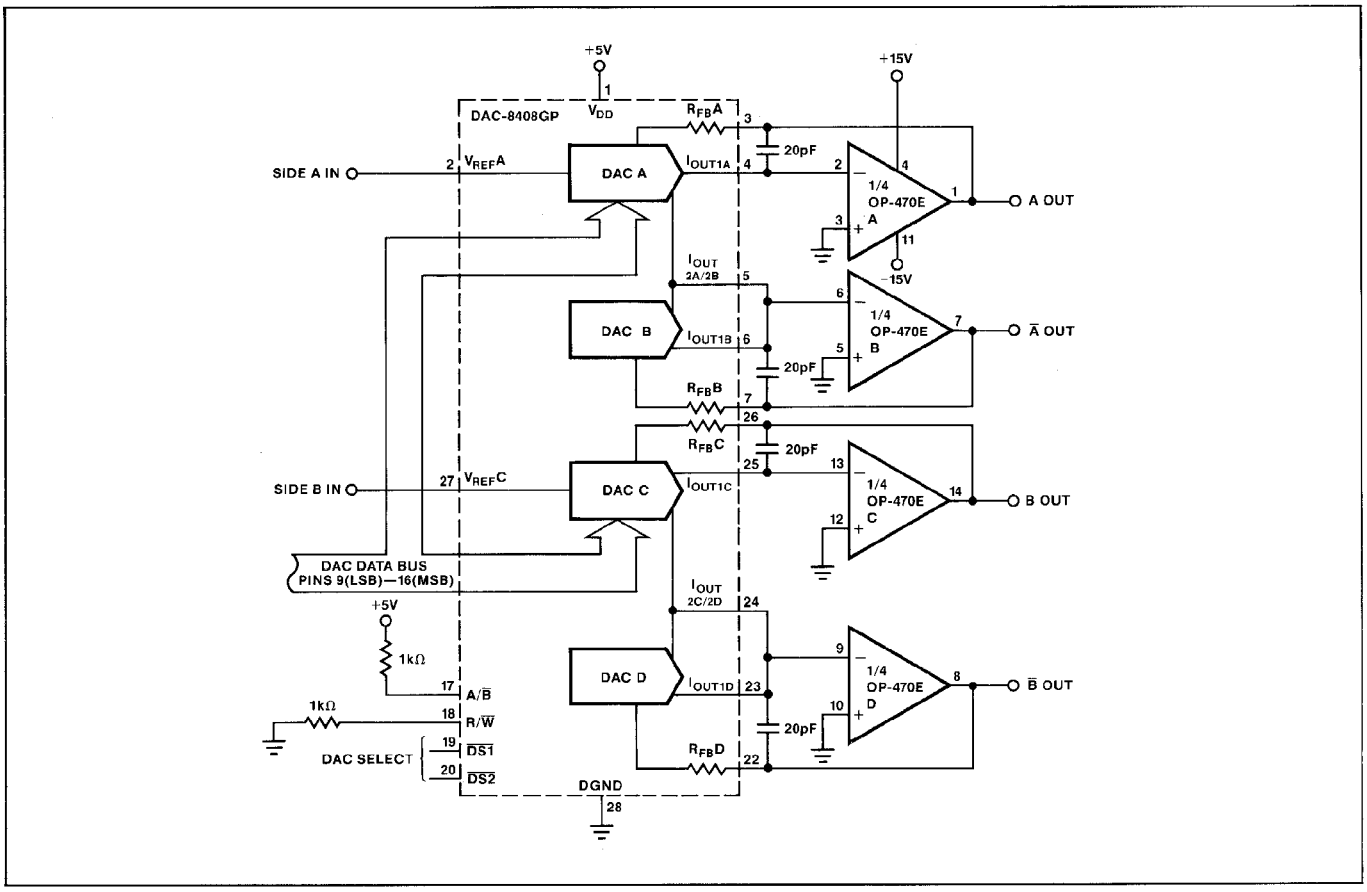


FIGURE 13: Digital Panning Control Output

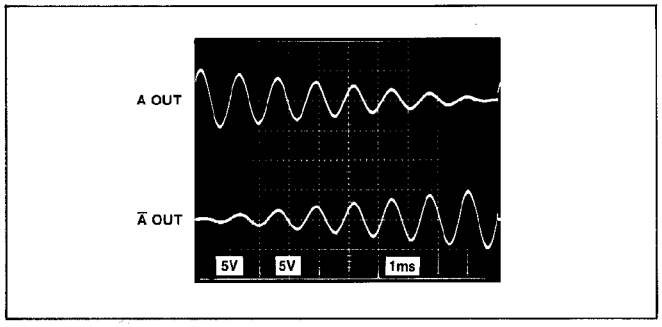
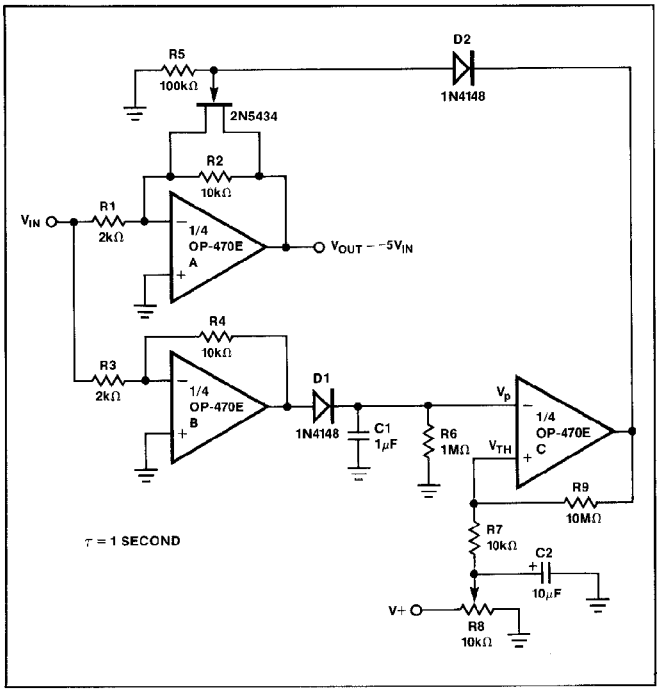


FIGURE 14: Squelch Amplifier



SQUELCH AMPLIFIER

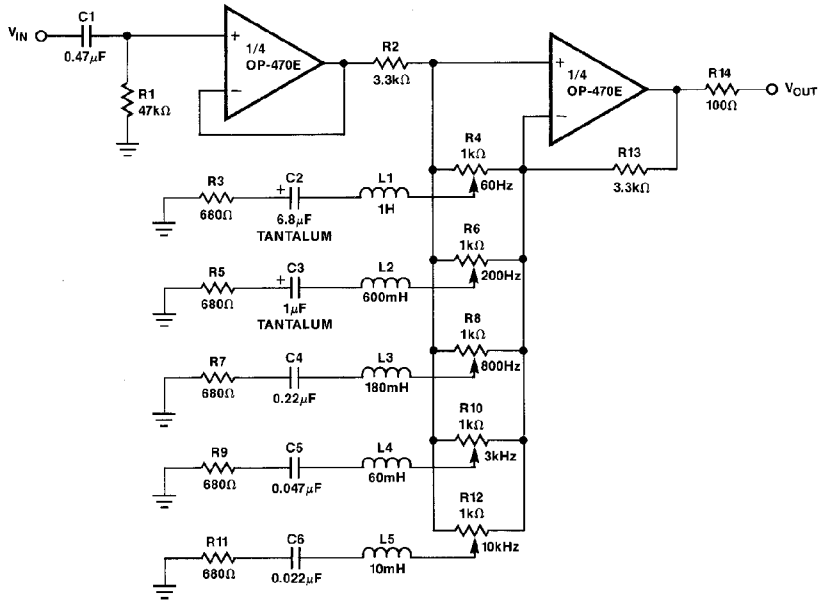
The circuit of Figure 14 is a simple squelch amplifier that uses a FET switch to cut off the output when the input signal falls below a preset limit.

The input signal is sampled by a peak detector with a time constant set by C1 and R6. When the output of the peak detector, V_p, falls below the threshold voltage, V_{TH}, set by R8, the comparator formed by op amp C switches from V− to V+. This drives the gate of the N-channel FET high, turning it ON, reducing the gain of the inverting amplifier formed by op amp A to zero.

FIVE-BAND LOW NOISE STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 15 provides 15dB of boost or cut over a 5-band range. Signal-to-noise ratio over a 20kHz bandwidth is better than 100dB referred to a 3V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

FIGURE 15: 5-Band Low Noise Graphic Equalizer



FREQUENCY MIXERS

Surface Mount

LEVEL 13 150 kHz to 6 GHz


ADE


ALY


† JMS


† LRMS-J

BLUE CELL™


MBA


MCA1

+13 dBm LO, up to +9 dBm RF

◆ MODEL NO.	FREQUENCY MHz LO/RF f_L-f_U	IF	CONVERSION LOSS dB Mid-Band $\bar{x}$	σ	Max.	Total Range Max.	LO-RF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	LO-IF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	IP3@ center band Typ. (dBm)	E factor	CASE STYLE	CONNECTION	PCB Lay-out PL-	PRICE $ Qty. (10-49)
◆ ADE-1MH**	2-500	DC-500	5.2	.10	6.5	8.0	60	45	50	35	48	25	55	40	45	30	40	22	17	0.4	CD542	ht	052	5.95
◆ ADE-1MHW**	0.5-600	DC-600	5.2	.10	6.9	8.0	63	50	53	32	43	20	56	40	44	25	30	20	17	0.4	CD636	ht	052	6.45
◆ ADE-10MH**	800-1000	10-200	7.0	0.2	—	8.5			34 (Typ.)		20 (Min.)				29 (Typ.)		20 (Min.)		26	1.3	CD636	ht	052	6.95
◆ ADE-12MH**	10-1200	DC-1200	6.3	.10	8.0	8.5	62	45	45	32	40	26	68	40	42	27	30	20	22	0.9	CD542	ht	052	6.45
◆ ADE-25MH**	5-2500	5-1500	6.9	.10	8.5	9.8	47	28	34	23	34	23	34	23	32	20	23	17	18	0.5	CD542	ht	052	6.95
◆ ADE-35MH**	5-3500	5-2500	6.9	.10	9.3	10.5	47	28	33	23	38	18	34	23	28	18	23	17	18	0.5	CD542	ht	052	9.95
◆ ADE-42MH**	5-4200	5-3500	7.5	.20	9.8	11.8	47	28	29	20	30	15	34	23	26	17	23	17	17	0.4	CD542	ht	052	14.95
◆ MBA-15MH*	1400-2400	DC-600	5.5	0.1	—	8.5			28 (Typ.)		16 (Min.)				16 (Typ.)		8 (Min.)		18	0.5	SM2	ld	066	7.95
◆ MBA-25MH*	2000-3000	DC-500	6.5	0.1	—	8.6			36 (Typ.)		18 (Min.)				20 (Typ.)		7 (Min.)		16	0.3	SM2	ld	066	7.95
NEW MCA1-24MH*	300-2400	DC-700	6.1	0.1	8.9				40		20				25		14		13	0	DZ885	ld	045	6.95
NEW MCA1-42MH*	1000-4200	DC-1500	6.2	0.1	8.9				32		20				20		10		16	0.3	DZ885	ld	045	7.95
NEW MCA1-60MH*	1600-4400	DC-2000	6.9	0.1	8.5				32		25				17		—		15	0.2	DZ885	ld	045	8.95
	4400-6000	DC-2000	6.0	0.1	8.5				22		18				15		—		15	0.2				
◆ ALY-44MH	2400-4400	DC-1400	7.5	.20	—	8.9			30 (Typ.)		20 (Min.)				20 (Typ.)		10 (Min.)		—		CB518	jy	085	18.95
◆ ALY-44MHW	1800-4900	DC-1400	7.5	.20	—	9.2			30 (Typ.)		20 (Min.)				14 (Typ.)		8 (Min.)		—		CB518	jy	085	19.95
JMS-1MH	2-500	DC-500	5.75	.10	7.0	8.0	70	55	60	40	44	25	55	42	45	25	35	20	—		BH292	ht	052	9.45
JMS-2MH	20-1000	DC-1000	7.0	.15	8.4	9.5	63	40	50	28	35	20	56	30	47	22	37	20	—		BH292	ht	052	10.45
JMS-5MH	5-1500	DC-1000	5.7	.10	8.0	9.5	67	40	57	25	35	20	60	40	35	18	15	8	—		BH292	ht	052	11.95
◆ LRMS-1MHJ	2-500	DC-500	5.65	.08	7.0	8.0	58	45	44	25	30	20	55	40	36	25	28	17	—		QQQ569	w	083	8.95
◆ LRMS-2MHJ	5-1000	DC-1000	6.72	.08	8.5	9.5	55	40	39	20	22	16	52	35	30	17	18	12	—		QQQ569	w	083	9.95
◆ LRMS-2UMHJ	10-1000	20-500	7.0	.10	8.5	9.5	52	40	43	30	33	25	53	30	44	25	39	22	—		QQQ569	w	083	14.45
◆ LRMS-5MHJ	10-1500	DC-900	5.67	.09	9.0	9.5	58	40	40	20	26	18	50	30	38	18	17	8	—		QQQ569	w	083	15.95

E= [IP3(dBm)-LO Power(dBm)]/10

L = low range [f_L to 10 f_L] M = mid range [10 f_L to f_U/2] U = upper range [f_U/2 to f_U]

m = mid band [2f_L to f_U/2]

NOTES:

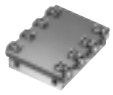
$\bar{x}$ Average of conversion loss at center of mid-band frequency (f_L+f_U/4)
σ Standard deviation
◆ Aqueous washable. For non-aqueous requirements, LRMS units available in case style QQQ130.
❑ Non-hermetic
† Phase detection, positive polarity
‡ Conversion loss increases up to 6 dB higher as IF frequency decreases from 5 MHz to DC.
✪ Frequency Specified RMS-42MH m=1000 - 2000 MHz, L=800 - 2100 MHz, U=2100 - 4200 MHz; TUF-2MHSM L=50-100 MHz M=100-500 MHz
* BLUE CELL™ mixers protected by U.S. Patents 5,534,830 5,640,132 5,640,134 5,640,699
** Protected under U.S. Patent 6133525
*** Prices for quantities 10-49
A. Environmental specifications and re-flow soldering information available in General Information Section.
B. Units are non-hermetic unless otherwise noted. For details on case dimensions & finishes see "Case Styles & Outline Drawings".
C. Prices and Specifications subject to change without notice.
1. Absolute maximum power, voltage and current ratings: 1a. RF power 200mW; 1b. Peak IF current, 40mA

NSN GUIDE

MCL NO.	NSN
ROK-186MH	5895-01-392-2276
SRA-1MH	5895-01-391-0113
TFM-3MH	5895-01-302-7047
TFM-42MH	5895-01-408-6093

020729


† RMS


SKY


SYM


TUF-SM

+13 dBm LO, up to +9 dBm RF

◆ MODEL NO.	FREQUENCY MHz LO/RF f_L-f_U	IF	CONVERSION LOSS dB Mid-Band m $\bar{x}$	σ	Max.	Total Range Max.	LO-RF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	LO-IF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	IP3@ center band Typ. (dBm)	E factor	CASE STYLE	CONNECTION	PCB Lay-out PL-	PRICE $ Qty. (10-49)
RMS-1MH	2-500	DC-500	5.65	.08	7.0	8.0	58	45	44	25	30	20	55	40	36	25	28	17	26	1.3	TT240	w	052	8.95
RMS-2MH	5-1000	DC-1000	6.72	.08	8.5	9.5	55	40	39	20	22	16	52	35	30	17	18	12	—		TT100	w	052	9.95
RMS-5MH	10-1500	DC-900	5.67	.09	9.0	9.5	58	40	40	20	26	18	50	30	38	18	17	8	—		TT240	w	052	15.95
RMS-25MH	5-2500	5-1500	7.0	.20	8.5	9.8	54	28	32	23	32	20	34	23	32	25	28	17	17	0.4	TT240	w	052	9.95
NEW RMS-25MHW	5-2500	5-2200	7.0	0.1	8.5	9.8	54	28	32	23	32	20	34	23	32	25	28	17	17	0.4	TT240	w	052	7.95
JRMS-42MH	800-4200	DC-800	5.3	.20	9.0	10.8	35	25	—	—	28	17	18	10	—	—	15	7	—		TT240	w	052	24.95
SKY-53MHR	2800-5300	DC-500	5.7	.20	—	9.5	28 (Typ.)	15 (Min.)					12 (Typ.)	8 (Min.)					19	0.6	BJ398	hp		17.95
SKY-60MH	2500-6000	DC-1500	6.2	.20	—	9.5	28 (Typ.)	17 (Min.)					14 (Typ.)	8 (Min.)					19	0.6	BJ398	je		17.95
SYM-11MH	50-2000	50-1000	6.6	.10	8.0	9.9	55	35	44	25	30	20	40	25	36	20	29	20	—		TTT167	x		15.95
SYM-25DMHW	40-2500	DC-1000‡	6.6	.10	8.0	9.0	47	32	37	27	35	22	38	28	35	25	38	20	26	1.3	TTT167	x		8.95***
SYM-1020MH	1000-2000	DC-800	6.5	.55	—	9.8	32 (Typ.)	20 (Min.)					20 (Typ.)	10 (Min.)					18	0.5	TTT167	lq		9.95
SYM-8022MH	800-2200	DC-800	7.6	0.3	—	9.8	26 (Typ.)	18 (Min.)					20 (Typ.)	9 (Min.)					18	0.5	TTT167	lp		11.95
TUF-1MHSM	2-600	DC-600	6.3	.12	7.0	8.0	68	50	50	30	43	25	65	45	48	30	37	22	15	0.2	NNN150	z		8.25
✪ TUF-2MHSM	50-1000	DC-1000	6.0	.25	7.5	9.0	58	40	47	30	37	25	55	35	47	20	32	18	—		NNN150	z		9.20
TUF-3MHSM	0.15-400	DC-400	5.0	.33	7.0	8.0	60	50	46	30	35	25	60	40	42	25	35	20	—		NNN150	z		10.20
TUF-5MHSM	20-1500	DC-1000	7.0	.25	8.5	9.0	50	40	41	30	35	25	38	25	28	18	20	8	—		NNN150	z		13.45
TUF-11AMHSM	1400-1900	40-500	7.4	.20	8.6	8.6	33 (Typ.)	20 (Min.)					24 (Typ.)	15 (Min.)					—		NNN150	z		21.95
TUF-2500MHSM	400-2500	30-800	7.3	.15	8.5	10.0	32 (Typ.)	24 (Min.)					27 (Typ.)	17 (Min.)					—		NNN150	z		21.95

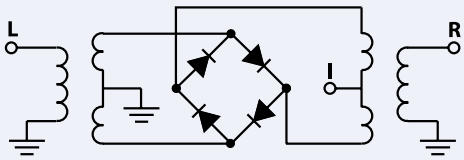
E= [IP3(dBm)-LO Power(dBm)]/10

L = low range [f_L to 10 f_L]

M = mid range [10 f_L to f_U/2]

m = mid band [2f_L to f_U/2]

U = upper range [f_U/2 to f_U]



pin and coaxial connections see case style outline drawings

PORT	w	x	z	hp	ht	je	jy	lc	ld	lp	lq
LO	1	2	4	5	6	1	1	10	10	3	3
RF	4	1	1	1	3	5	6	5	5	1	2
IF	5	3	2	7	2	7	10	3	3	2	1
GND EXT.	2,3,6	4,5,6	3	2,3,4,6,8	1,4,5	2,3,4,6,8	all others	1,4,7,8,9	1,2,4,6,7,8,9	4,5,6	4,5,6
ISOLATE	—	—	—	—	—	—	—	2,6	—	—	—
DEMO BOARD	TB-03	TB-12	—	TB-11	TB-03	TB-11	—	TB-117	TB-99 (MBA) TB-144 (MCA1)	—	—

020729

MONOLITHIC AMPLIFIERS 50Ω

BROADBAND DC to 8 GHz


ERA


ERA-SM

low power, up to +13.5 dBm output

all specifications at 25°C

MODEL◆ NO.	✪ FREQ. GHz f_L - f_u	GAIN, dB Typical over frequency, GHz 0.1	1	2	3	4	6	8	Min.@ 2 GHz	Flatness DC-2 GHz	MAXIMUM POWER (dBm) at 2 GHz* Output (1 dB Comp.) Typ.	Min.	Input (no dmg)	DYNAMIC RANGE at 2 GHz* NF (dB) Typ.	IP3 (dBm) Typ.	VSWR (:1) Typ. In DC-3 GHz	3-f_u** GHz	Out DC-3 GHz	3-f_u** GHz	ABSOLUTE MAX. RATING[3] I (mA)	P (mW)	DC OPERATING POWER[4] at Pin 3 Current (mA)	Volt. Typ	Min	Max	THERMAL RESISTANCE θjc Typ. °C/W	CASE STYLE Note B	CONNECTION	PRICE $ Qty. (30)
ERA-1	DC-8	12.3	12.1	11.8	10.9	9.7	7.9	8.2	9	±0.3	12.0	10.0	15	4.3	26	1.5	1.8	1.5	1.9	75	330	40	3.4	3.0	4.1	178	VV105	cb	1.37
ERA-2	DC-6	16.2	15.8	15.2	14.4	13.1	11.2	—	13	±0.5	13.0	11.0	15	4.0	26	1.3	1.4	1.2	1.6	75	330	40	3.4	3.0	4.1	155	VV105	cb	1.52
ERA-3	DC-3	22.1	21.0	18.7	16.8	—	—	—	16	±1.7	12.5	9	13	3.5	25	1.5	—	1.4	—	75	330	35	3.2	3.0	4.1	154	VV105	cb	1.67
ERA-1SM	DC-8	12.3	12.1	11.8	10.9	9.7	7.9	8.2	9	±0.3	12.0	10.0	15	4.3	26	1.5	1.8	1.5	1.9	75	330	40	3.4	3.0	4.1	183	WW107	cb	1.42
NEW ERA-21SM	DC-8	14.2	13.9	13.2	12.2	10.8	8.7	8.9	11.2	±0.5	12.6	10.6	15	4.7	26	1.1	1.4	1.3	1.9	75	330	40	3.5	3.0	4.1	194	WW107	cb	1.57
ERA-2SM	DC-6	16.2	15.8	15.2	14.4	13.1	11.2	—	13	±0.5	13.0	11.0	15	4.0	26	1.3	1.4	1.2	1.6	75	330	40	3.4	3.0	4.1	160	WW107	cb	1.57
NEW ERA-33SM	DC-3	19.3	18.7	17.4	15.9	—	—	—	15	±0.9	13.5	11.5	13	3.9	28.5	1.6	—	1.25	—	75	330	40	4.3	3.8	4.8	140	WW107	cb	1.72
ERA-3SM	DC-3	22.1	21.0	18.7	16.8	—	—	—	16	±1.7	12.5	9	13	3.5	25	1.5	—	1.4	—	75	330	35	3.2	3.0	4.1	159	WW107	cb	1.72

features

- low thermal resistance
- miniature microwave amplifier
- available in drop-in & surface mount (sm) versions
- frequency range, DC to 8 GHz, usable to 10 GHz
- up to 18.5 dBm typ. (16.5 dBm min) output power

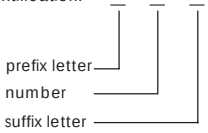
absolute maximum ratings

operating temperature: -45°C to 85°C
storage temperature: -65° to 150°C

model identification

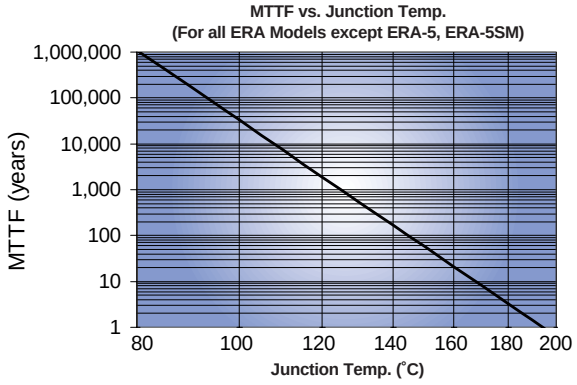
Model	marking (see note below)
ERA-1, ERA-1SM	1
ERA-2, ERA-2SM	2
ERA-21SM	21
ERA-3, ERA-3SM	3
ERA-33SM	33
ERA-4, ERA-4SM	4
ERA-5, ERA-5SM	5
ERA-50SM	50
ERA-51SM	51
ERA-6, ERA-6SM	6

Note: Prefix letter (optional) designates assembly location. Suffix letters (optional) are for wafer identification.



NOTES:

◆ Aqueous washable
* at 1 GHz for ERA-4,5,6, 4SM, 5SM, 50SM, 51SM, 6SM
** f_u is the upper frequency limit for each model as shown in the table.
*** Gain, gain flatness, and VSWR are specified at 1.5 GHz.
✪ Low frequency cutoff determined by external coupling capacitors.
A. Environmental specifications and re-flow soldering information available in General Information Section.
B. Units are non-hermetic unless otherwise noted. For details on case dimensions & finishes see "Case Styles & Outline Drawings".
C. Prices and Specifications subject to change without notice.
D. For Quality Control Procedures see Table of Contents, Section 0, "Mini-Circuits Guarantees Quality" article. For Environmental Specifications see Amplifier Selection Guide.
1. Model number designated by alphanumeric code marking.
2. ERA-SM models available on tape and reel.
3. Permanent damage may occur if any of these limits are exceeded. These ratings are not intended for continuous normal operation.
4. Reliability predictions and normal operating conditions are applicable at current specified.



REV. G
M77341
ERA-SERIES
RD/YB/FL
010621
Page 1 of 2

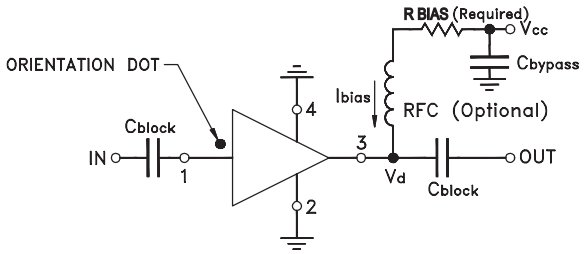
Mini-Circuits®
INTERNET http://www.minicircuits.com
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661
Distribution Centers NORTH AMERICA 800-654-7949 • 417 335-5935 • Fax 417-335-5945 • EUROPE 44-1252-832600 • Fax 44-1252-837010
ISO 9001 CERTIFIED

medium power, up to +18.4 dBm output

all specifications at 25°C

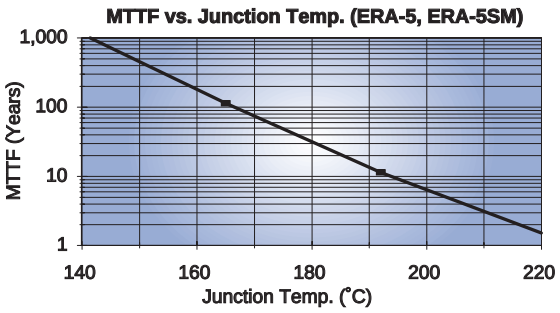
MODEL◆ NO.	FREQ. GHz f_L - f_u	GAIN, dB Typical over frequency, GHz 0.1	1	2	3	4	6	8	Flatness Min.@ 2 GHz	Flatness DC-2 GHz	MAXIMUM POWER (dBm) at 2 GHz* Output (1 dB Comp.) Typ.	Min.	Input (no dmg)	DYNAMIC RANGE at 2 GHz* NF (dB) Typ.	IP3 (dBm) Typ.	VSWR (:1) Typ. In DC-3 GHz	In 3-f_u** GHz	Out DC-3 GHz	Out 3-f_u** GHz	ABSO-LUTE MAX. RATING[3] I (mA)	P (mW)	DC OPERATING POWER[4] at Pin 3 Current (mA)	Volt. Typ	Min	Max	THERMAL RESIS-TANCE θjc Typ. °C/W	CASE STYLE Note B	CONNECTION	PRICE $ Qty. (30)
ERA-6	DC-4	12.6	12.5	12.2	11.7	11.3	—	—	10.5	±0.2	17.9	16	20	4.5	36	1.3	1.2	1.6	1.8	120	650	70	5.0	4.6	5.6	170	VV105	cb	3.85
ERA-4	DC-4	14.3	14.0	13.4	12.7	11.8	—	—	11	±0.4	17.3	15	20	4.2	34	1.2	1.2	1.3	1.8	120	650	65	4.5	4.2	5.5	163	VV105	cb	3.85
ERA-5	DC-4	20.2	19.5	18.5	17.3	16.2	—	—	16	±1.0	18.4	16.5	13	4.3	32.5	1.3	1.3	1.2	1.3	120	650	65	4.9	4.2	5.5	278	VV105	cb	3.85
ERA-6SM	DC-4	12.6	12.5	12.2	11.7	11.3	—	—	10.5	±0.2	17.9	16	20	4.5	36	1.3	1.2	1.6	1.8	120	650	70	5.0	4.6	5.6	175	WW107	cb	3.90
ERA-4SM	DC-4	14.3	14.0	13.4	12.7	11.8	—	—	11	±0.4	17.3	15	20	4.2	34	1.2	1.2	1.3	1.8	120	650	65	4.5	4.2	5.5	168	WW107	cb	3.90
NEW ERA-51SM	DC-4	18.0	17.4	16.1	14.8	12.5	—	—	14	±1.0	18.1	16.5	13	4.1	33	1.1	1.2	1.2	1.9	120	650	65	4.5	4.2	5.5	154	WW107	cb	3.90
ERA-5SM	DC-4	20.2	19.5	18.5	17.3	16.2	—	—	16	±1.0	18.4	16.5	13	4.3	32.5	1.3	1.3	1.2	1.3	120	650	65	4.9	4.2	5.5	283	WW107	cb	3.90
NEW ERA-50SM***	DC-1.5	20.7	19.4	18.3	—	—	—	—	16	±1.2	17.2	16.0	13	3.5	32.5	1.3	—	1.2	—	120	650	60	4.4	4.0	4.9	177	WW107	cb	2.95

typical biasing configuration



R BIAS
"1%" Resistor Values (ohms) for Optimum Biasing of ERA Models

Vcc	ERA-1, 1SM	ERA-2, 2SM	ERA-21SM	ERA-3, 3SM	ERA-33SM	ERA-4, 4SM	ERA-5, 5SM	ERA-50SM, 51SM	ERA-6, 6SM
7	90.9	88.7	88.7	107	69.8	38.3	40.2	40.2	30.1
8	113	113	113	133	93.1	52.3	53.6	53.6	43.2
9	137	137	137	162	115	66.5	68.1	68.1	56.2
10	162	162	162	191	140	80.6	82.5	82.5	69.8
11	187	187	187	221	165	95.3	97.6	97.6	84.5
12	215	215	210	249	191	110	113	113	97.6
13	237	237	237	280	215	127	127	127	113
14	261	261	261	309	243	143	143	143	127
15	287	287	287	340	267	158	158	158	140
16	309	316	316	365	287	174	174	174	154
17	332	340	340	392	316	187	191	191	169
18	357	365	365	422	340	205	205	205	182
19	383	392	392	453	365	221	221	221	196
20	412	412	412	475	392	237	237	237	210



designers kits available

KIT NO.	Model Type	No. of Units in Kit	Description	Price $ per kit
K1-ERA	ERA	30	10 of each 1,2,3	49.95
K2-ERA	ERA	20	10 of each 4,5	69.95
K1-ERASM	ERA-SM	30	10 of each 1SM, 2SM,3SM	49.95
K2-ERASM	ERA-SM	20	10 of each 4SM, 5SM	69.95
K3-ERASM	ERA-SM	30	10 of each 4SM, 5SM, 6SM	99.95

pin connections

PORT	cb
RF IN	1
RF OUT	3
DC	3
CASE GND	2,4
NOT USED	—

NSN GUIDE

MCL NO.	NSN
ERA-1SM	5962-01-459-9075
ERA-2SM	5962-01-459-7410
ERA-3SM	5962-01-459-9314

VOLTAGE CONTROLLED OSCILLATORS

Click package to view outline drawing

165S

SURFACE-MOUNT PACKAGE

FREQUENCY RANGE (MHz)	NOMINAL TUNING VOLTAGE (Volts)	DC BIAS REQUIREMENTS VOLTAGE (Volts)	DC BIAS REQUIREMENTS CURRENT (mA)	OUTPUT POWER dBm	OUTPUT POWER Tolerance (dB)	AVERAGE TUNING SENSITIVITY MHz/Volt	TYPICAL PHASE NOISE dBc/Hz Offset at 10 KHz/100 KHz	TYPICAL HARMONIC SUPPRESSION (dBc)	PUSHING (MHz/Volt) (Typ)	PULLING (@ 1.75:1 VSWR) MHz (Typ)	MODEL
180 - 260	0 - 10	+12	<30	+7.5	+2	8 - 15	-95/-120	10	1	15	**VFC180SA**
200 - 400	0 - 17	+12	<35	+14	+2.5	10 - 20	-90/-115	10	5	15	**VFC-S-200**
210 - 270	1 - 12	+5.0	<35	0	+2	5 - 6	-90/-115	10	5	15	**VFC210SA**
219 - 256	1 - 4.5	+5	<20	0	+2	12 - 20	-100/-120	10	5	5	**VFC219SA**
250 - 500	0 - 22	+12	<35	+12	+2.5	10 - 20	-95/-115	10	5	15	**VFC-S-250**
400 - 800	0 - 15	+12	<35	+12	+2.5	20 - 30	-95/-115	10	5	15	**VFC-S-400**
425 - 500	1 - 12	+12	<35	+10	+3	5 - 10	-95/-120	10	5	15	**VFC-S-A05**
490 - 560	0 - 4.5	+8	<20	0	+2	17 - 25	-100/-125	10	1	2	**VFC490SA**
500 - 1000	0.5 - 25	+12	<35	+14	+2.5	25 - 50	-95/-120	10	1	15	**VFC-S-500**
600 - 1200	0.5 - 25	+12	<35	+15	+3	25 - 45	-95/-115	10	1	15	**VFC-S-600**
700 - 1400	0.5 - 25	+12	<35	+15	+3	35 - 60	-95/-120	10	5	15	**VFC-S-700**
800 - 1600	0 - 25	+12	<35	+14	+3.5	40 - 60	-95/-120	10	5	15	**VFC-S-800**
900 - 1200	2.5 - 10.5	+12	<35	+6	+1.5	40 - 60	-95/-120	10	5	15	**VFC900SB**
900 - 1735	0 - 18	+15	<45	+13	+1.5	40 - 60	-95/-120	10	5	16	**VFC900SA**
900 - 1800	0.5 - 20	+12	<35	+11	+3	40 - 60	-95/-120	10	5	15	**VFC-S-900**
920 - 1455	0 - 12	+12	<35	+13	+3	45 - 60	-95/-120	10	5	15	**VFC920SA**
936 - 1636	0 - 20	+12	<35	+10	+3	20 - 50	-90/-115	10	5	15	**VFC 936SA**
1000 - 2000	0.5 - 22	+12	<35	+13	+3	40 - 60	-95/-120	10	5	15	**VFC-S-1000**
1200 - 1600	2.5 - 11	+12	<35	+6	+1.5	50 - 70	-95/-120	10	5	15	**VFC1200SA**
1225 - 2375	0 - 25	+11	<35	+12	+4	50 - 70	-95/-120	10	2	30	**VFC1225SA**
1300 - 2300	0 - 24	+15	<40	+12	+3	40 - 60	-90/-110	10	1	15	**VFC1300SA**
1305 - 1512	2 - 10	+12	<30	+10	+1	20 - 40	-95/-120	20	5	15	**VFC-S-A07**
1355 - 1595	2 - 10	+12	<30	+10	+1	25 - 45	-95/-115	10	1	15	**VFC-S-A06**
1500 - 2100	1 - 12	+12	<35	+6	+2.5	40 - 60	-92/-112	10	5	15	**VFC-S-A02**
1850 - 1950	0.5 - 6.5	+8	<40	+8	+2	20 - 30	-95/-122	12	3.5	15	**VFC1850SA**
2300 - 2450	0.5 - 7	+8	<35	+8	+2	25 - 35	-95/-120	12	3.5	20	**VFC2300SA**
2355 - 2528	0.5 - 4.5	+12	<35	+5	+3	50 - 60	-90/-115	10	5	10	**VFC2355SA**
2530 - 2730	1 - 9	+12	<35	+10	+2	30 - 45	-90/-120	20	5	15	**VFC2530SA**

COMMON SPECIFICATIONS

Output Impedance: 50 ohms
VSWR: 1.5:1 (Typ)
Specifications are at +25°C

Operating Temperature: -30°C to +70°C
Contact the factory for more stringent operating temperature range

For pin location and package outline drawings, see back pages.

201 McLean Boulevard • Paterson, New Jersey 07504 • Tel: (973) 881-8800 • Fax: (973) 881-8361
E-Mail: sales@synergymwave.com • World Wide Web: http://www.synergymwave.com

SYNERGY® MICROWAVE CORPORATION

VOLTAGE CONTROLLED OSCILLATORS

PLUG-IN PACKAGE

165

FREQUENCY RANGE (MHz)	NOMINAL TUNING VOLTAGE (Volts)	DC BIAS REQUIREMENTS VOLTAGE (Volts)	DC BIAS REQUIREMENTS CURRENT (mA)	OUTPUT POWER dBm	OUTPUT POWER Tolerance (dB)	AVERAGE TUNING SENSITIVITY MHz/Volt	TYPICAL PHASE NOISE dBc/Hz Offset at 10 KHz/100 KHz	TYPICAL HARMONIC SUPPRESSION (dBc)	PUSHING (MHz/Volt) (Typ)	PULLING (@ 1.75:1 VSWR) MHz (Typ)	MODEL
200 - 400	0 - 17	+12	<35	+14	+2.5	10 - 20	-90/-115	10	5	15	**VFC-P-200**
250 - 500	0 - 22	+12	<35	+12	+2.5	10 - 20	-95/-115	10	5	15	**VFC-P-250**
400 - 800	0.5 - 15	+12	<35	+15	+2.5	20 - 30	-95/-115	10	1	15	**VFC-P-400**
500 - 1000	0.5 - 25	+12	<35	+14	+2.5	25 - 50	-95/-120	10	1	15	**VFC-P-500**
600 - 1200	0.5 - 25	+12	<35	+15	+3	25 - 45	-95/-115	10	1	15	**VFC-P-600**
700 - 1400	0.5 - 25	+12	<35	+15	+3	35 - 60	-95/-120	10	5	15	**VFC-P-700**
800 - 1600	0 - 25	+5	<35	+10	+3	40 - 60	-95/-120	10	1	15	**VFC-P-800**
900 - 1800	0.5 - 20	+12	<35	+11	+3	40 - 60	-95/-120	10	5	15	**VFC-P-900**
1000 - 2000	0.5 - 22	+12	<35	+11	+3	40 - 60	-95/-120	10	5	15	**VFC-P-1000**
1630 - 1930	2 - 22	+10	<50	+10	+2	15 - 30	-95/-115	10	5	15	**VFC-P-A02**

COMMON SPECIFICATIONS

Output Impedance: 50 ohms
VSWR: 1.5:1 (Typ)
Specifications are at +25°C

Operating Temperature: -30°C to +70°C
Contact the factory for more stringent operating temperature range

For pin location and package outline drawings, see back pages.

201 McLean Boulevard • Paterson, New Jersey 07504 • Tel: (973) 881-8800 • Fax: (973) 881-8361
E-Mail: sales@synergymwave.com • World Wide Web: http://www.synergymwave.com

SYNERGY® MICROWAVE CORPORATION

FREQUENCY DOUBLERS 50Ω Surface Mount ❑

HIGH HARMONIC REJECTION 50 kHz to 9600 MHz

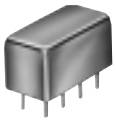
SURFACE MOUNT


KBA


SYK


SK


AK


RK


FD


FK

MODEL NO.	FREQUENCY MHz Input	Output	RF INPUT PWR dBm Min.	Max.	CONVERSION LOSS dB Input freq.	Typ.	Max.	❄HARMONIC OUTPUT dBc F1 Typ.	F1 Min.	F3 Typ.	F3 Min.	F4 Typ.	F4 Min.	CASE STYLE Note B	CONNECTION	PRICE $ Qty. (1-9)
◆ KBA-20*	1600-2200	3200-4400	11	15	1600-2200	12	15.8	12	7	20	13	23	10	SM2	ln	9.95***
◆ KBA-40*	2700-4800	5400-9600	10 5	16 10	2700-4800 2700-4800	12.3 13	17.6 19	18 15	10 8	26 26	15 16	24 26	14 12	SM2	ne	14.95
SYK-2R	10-1000	20-2000	12	16	10-500 500-1000	10.5 11.5	14.0 16.0	35 32	25 20	42 37	25 20	20 20	10 10	TTT167	gc	29.95
SK-2	1-500	2-1000	1	10	1-100 100-300 300-500	13.0 13.5 14.0	15.0 15.5 17.5	40 25 20	30 20 15	50 40 30	40 30 25	16 16 16	12 12 12	B02	df	26.45
AK-2	1-500	2-1000	1	10	1-100 100-300 300-500	13.0 13.5 14.0	15.0 15.5 17.5	40 25 20	30 20 15	50 40 30	40 30 25	16 16 16	12 12 12	A03	dg	20.95
AK-3000	70-1500	140-3000	12	15	70-1000 1000-1500	10.5 11.5	14.0 16.0	31 22	20 15	40 30	25 20	14 30	10 14	A03	ga	59.95
RK-2	5-500	10-1000	1	15	5-100 100-300 300-500	13.0 13.5 14.0	16.0 15.5 16.5	40 25 20	30 20 15	50 40 30	40 30 25	16 16 16	12 12 12	A01	dg	17.95
RK-3	0.05-150	0.1-300	0	13	0.05-50 50-150	11.0 11.5	17.0 15.0	40 35	28 20	45 40	30 20	16 16	8 12	A01	dh	15.95
RK-5	10-800	20-1600	10	20	10-100 100-400 400-800	13.0 12.5 13.0	15.0 16.0 16.0	20 20 20	12 12 12	25 30 25	20 20 18	15 15 15	12 12 10	A01	dg	49.95
RK-3000	70-1500	140-3000	12	15	70-1000 1000-1500	11.0 12.0	14.0 17.5	31 22	20 15	40 30	25 20	15 30	10 14	A01	ga	54.95
FD-2	5-500	10-1000	1	15	5-100 100-300 300-500	13.0 13.5 14.0	16.0 15.5 16.5	40 25 20	30 20 15	50 40 30	40 30 25	16 16 16	12 12 12	FF55	-	40.95
FK-5	10-1000	20-2000	10**	20	10-600 600-1000	13.0 14.0	15.0 17.0	20 20	10 10	16 25	20 20	15 25	10 15	H16	-	69.95
▲ FK-3000	70-1500	140-3000	12	15	70-1000 1000-1500	11.0 12.0	14.0 17.5	31 22	20 15	40 30	25 20	15 30	10 14	H16	-	79.95

NOTES:
- ◆ Aqueous washable
- ❑ Non-hermetic
- ❄ Harmonic output below power level of F2
- * BLUE CELL™ mixers protected by U.S. Patents 5,534,830 5,640,132 5,640,134 5,640,699
- ** Minimum input power +13 dBm above 700 MHz
- *** Price for quantities 10-49
- ▲ Available only with SMA connectors
- A. General Quality Control Procedures, Environmental Specifications, Hi-Rel and MIL description are given in General Information (section 0).
- B. Connector types and case mounted options, case finishes are given in section 0, see "Case Styles & Outline Drawings".
- C. Prices and Specifications subject to change without notice.
- 1. Absolute maximum power, voltage and current rating:
  1a. RF Input power, 200mW
  1b. FD-2 input is at Male BNC.

BLUE CELL™

020614

LK

MK

GK

MODEL NO.	FREQUENCY MHz		RF INPUT PWR dBm		CONVERSION LOSS dB			❄HARMONIC OUTPUT dBc						CASE STYLE	CONNECTION	PRICE $
								F1		F3		F4				
	Input	Output	Min.	Max.	Input freq.	Typ.	Max.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Note B		Qty. (1-9)
LK-3000	70-1500	140-3000	12	15	70-1000	10.5	14.0	31	20	40	25	15	10	BB48	dk	64.95
					1000-1500	11.5	16.0	22	15	35	20	20	14			
MK-2	5-500	10-1000	1	15	5-100	13.0	16.0	40	30	50	40	16	12	L19	-	52.95
					100-300	13.5	15.5	25	20	40	30	16	12			
					300-500	14.0	16.5	20	15	30	25	16	12			
MK-3	0.05-150	0.1-300	0	13	0.05-50	11.0	17.0	40	28	45	30	16	8	L19	-	47.95
					50-150	11.5	15.0	35	20	40	20	16	12			
MK-5	10-1000	20-2000	10**	20	10-600	13.0	15.0	20	10	26	20	15	10	L19	-	76.95
					600-1000	14.0	17.0	20	10	25	20	25	15			
GK-5	10-1000	20-2000	10**	20	10-600	13.0	15.0	20	10	26	20	15	10	L20	-	67.95
					600-1000	14.0	17.0	20	15	25	20	25	15			

pin connections

see case style outline drawings for pin locations

PORT	df	dg	dh	dk	ga	gc	ln	ne
INPUT	1,2 ^	1,3,4 ^	1,3,4 ^	4	1	2	10	10
OUTPUT	4	8	8	8	8	1	5	6
GND EXT.	3	2,5,6,7	2,5,6,7	1,2,3,5,6,7	2,3,4,5,6,7	4,5,6	1,2,4,6,7,8,9	2,3,4,5,7,8,9
CASE GND	3	2,5,6,7	2	1,2,3,5,6,7	2,3,4,5,6,7	—	—	—
NOT USED	—	—	—	—	—	3	—	—
SAMPLE(1)	—	—	—	—	—	—	3	1

^pins must be connected together externally

(1) sample port output power, -10 dBc typ. Terminate in 50 ohms if not used.

NSN GUIDE

MCL NO.	NSN
AK-2	5895-01-131-4569
FD-2	5895-00-087-7925
FK-5	5985-01-204-9746
MK-3BR	5895-01-332-8582
RK-2	5895-01-268-7337
RK-3	5895-01-143-3726
RK-3-TX	5895-01-160-8656
RK-6	5895-01-450-3793
SK-2	6625-01-247-8425

001204