DIGISAT

Documents Constructeurs

Documents Constructeurs Composants :

- Antennes de réception satellite (document partiel)
- QPSK/BPSK Demodulator L 64706 (document partiel)
- Diode Varicap BB 133 (document partiel)
- Amplificateur Linéaire Intégré LM 833 (document partiel)
- Mémoire UT 621024 (document partiel)
- Mémoire M 27C4001 (document partiel)
- Mémoire AM 29F010 (document partiel)
- Mémoire ST 24C16

Documents relatifs au Bus I^2C :

- I^2C-bus Specification version 2.1 (document partiel)
- I^2C-bus Allocation table
- I^2C-bus Controller PCF8584 (document partiel)
- I^2C-bus Hi-Fi Stereo Audio Processor TDA8425 (document partiel)

ANTENNES DE RÉCEPTION SATELLITE

Antennes FOCUS PRIMAIRE — Montage Az-El

- Réflecteur monobloc en aluminium peint en blan mat, avec support-tripode pour la tête LNB *UEU-014* d'IKUSI.
- Chaque antenne est livrée en deux emballages correspondants au *Réflecteur* et au *Support*.

RCF-180 + SCF-180

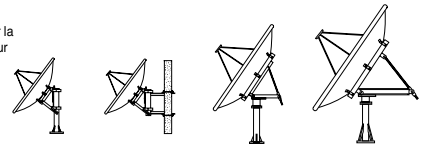
RÉFLECTEUR	Modèle	RCF-120	RCF-120	RCF-180	RCF-220
	Référence	1074	1074	1080	1075
SUPPORT	Modèle	SCF-120	STF-120	SCF-180	SCF-220
	Référence	1073	1072	1081	1076
Fixation		Sol	Pylone / Mur	Sol	Sol
Diamètre réflecteur	m	1,20		1,80	2,20
Bande satellite	GHz	10,7 - 12,75			
Gain (11,7 GHz)	dBi	41,4		44,9	46,7
Dynamique d'élévation	°	20 ... 70		25 ... 60	

Instructions de commande

- La commande d'une antenne doit spécifier la dénomination et la référence des Réflecteur et Support correspondants.

Exemple pour 1 antenne Ø1,80m:

- 1 RCF-180 (Réf. 1080)
- 1 SCF-180 (Réf. 1081)



RCF-120 + SCF-120 | RCF-120 + STF-120 | RCF-180 + SCF-180 | RCF-220 + SCF-220

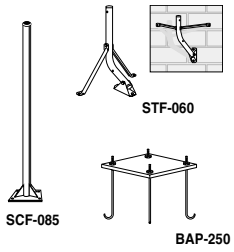
Antennes OFFSET — Montage Az-El

- Réflecteur acier galvanisé. Traitement de surface et double protection de polyester pour modèle «RPO». Protection de polyester pour «RPD» et «RPS».
- En modèles «RPD». pré-montés bras tête LNB et mécanisme de réglage d'élévation.

RPD-060

Modèle		RPO-100	RPD-085	RPD-060	RPS-040
Référence		3093	1084	1083	1064
Diamètre réflecteur	cm	100	85	60	40
Gain (11,7 GHz)	dBi	40,1	38,9	35,9	31,9
Angle "offset"	°	26			
Diamètre fixation tête SHF	mm	23 / 40	23 / 40	23 / 40	23
Fixation à mât de diamètre :	mm	30 à 75	32 à 60	32 à 60	30 à 60

Supports pour Antennes Satellite



SCF-085 | STF-060 | BAP-250

Modèle	Réf.	Description
SCF-085	1067	Fixation au sol. Type "colonne". Pour antennes *RPO-100* et *RPD-085*. Tube ø50 mm et platine quadrangulaire 200x200 mm en acier zingué chromé vert olive.
STF-085	1086	Fixation au sol ou mur. Type "tripode". Pour antennes *RPO-100* et *RPD-085*. Tube ø50 mm en acier galvanisé.
STF-060	1085	Fixation au sol ou mur. Type "tripode". Pour antennes *RPD-060* et *RPS-040*. Tube Ø40 mm en acier galvanisé.
BAP-200	1949	Platine d'ancrage pour la colonne *SCF-085*. Plaque 200x200x2 mm et 4 crochets M12.
BAP-250	1082	Platine d'ancrage pour les supports *SCF-120* et *SCF-180*. Plaque 250x250x2 mm et 4 crochets M16.
BAP-350	1077	Platine d'ancrage pour le support *SCF-220*. Plaque 350x350x2 mm et 4 crochets M18.

TÊTES LNB

Têtes 'QUATRO' pour des Antennes Collectives CE

- Deux modèles, pour montage sur antennes focus primaire et offset. Sont integrés LNB, source et transducteur orthomode.
- 4 sorties BIS (H-basse, H-haute, V-basse et V-haute). Raccordements F.

UEU-014

UEU-124K

Modèle		UEU-014	UEU-124K
Référence		3230	1114
Type d'antenne		focus primaire	offset
Fréquence d'entrée	GHz	10,7 - 12,75	
Nombre de sorties BIS		4 (2H - 2V)	
BIS aux deux sorties H (Bandes d'entrée rattachées)	MHz	950 - 1950 (10,7 - 11,7 GHz) / 1100 - 2150 (11,7 - 12,75 GHz)	950 - 1950 (10,7 - 11,7 GHz) / 1100 - 2150 (11,7 - 12,75 GHz)
BIS aux deux sorties V (Bandes d'entrée rattachées)	MHz	950 - 1950 (10,7 - 11,7 GHz) / 1100 - 2150 (11,7 - 12,75 GHz)	950 - 1950 (10,7 - 11,7 GHz) / 1100 - 2150 (11,7 - 12,75 GHz)
Gain	dB	55 (±5)	56 (±6)
Facteur de bruit (typ)	dB	0,7	0,7
Polarisation croisée	dB	≥ 20	≥ 25
Fréquences oscillateurs locaux	GHz	9,75 / 10,6	
Bruit de phase max	dBc/Hz	1 kHz: -50 ,, 10 kHz: -75 ,, 100 kHz: -95	
Affaibliss. de réflexion sortie	dB	≥ 7,5	≥ 7,5
Tension téléalimentation (1)	Vcc	+11,5 ... +19	+11,5 ... +19
Consommation max	mA	300	230
Diamètre fixation	mm	—	40

(1) Par n'importe lequel des quatre ports de sortie.

Tête Universelle pour des Antennes Individuelles CE

- Pour montage sur antennes "offset". Sont integrés LNB, source et polarisateur.
- Commutation bandes basse/haute par ton. Commutation polarisation H/V par tension.
- 1 sortie BIS. Raccordement F.

UEU-121K

Modèle		UEU-121K
Référence		1113
Type d'antenne		offset
Fréquences d'entrée	GHz	10,7 - 12,75
BIS à la sortie (Bandes d'entrée rattachées)	MHz	950 - 1950 (10,7 - 11,7 GHz) / 1100 - 2150 (11,7 - 12,75 GHz)
Commutation bandes basse/haute		par ton 0 / 22 kHz (1)
Commutation H/V		par tension +16,0 ... +19,0 V / +11,5 ... +14,0 V (1)
Gain	dB	56 (±6)
Facteur de bruit (typ)	dB	0,7
Polarisation croisée	dB	≥ 30
Fréquences oscillateurs locaux	GHz	9.75 / 10.6
Bruit de phase max	dBc/Hz	1 kHz: -60 ,, 10 kHz: -80 ,, 100 kHz: -100
Affaibliss. de réflexion sortie	dB	≥ 7,5
Tension téléalimentation (1)	Vcc	+11,5 ... +19
Consommation max	mA	100
Diamètre fixation	mm	40

(1) Par le port de sortie.

QPSK/BPSK DEMODULATOR

L 74706

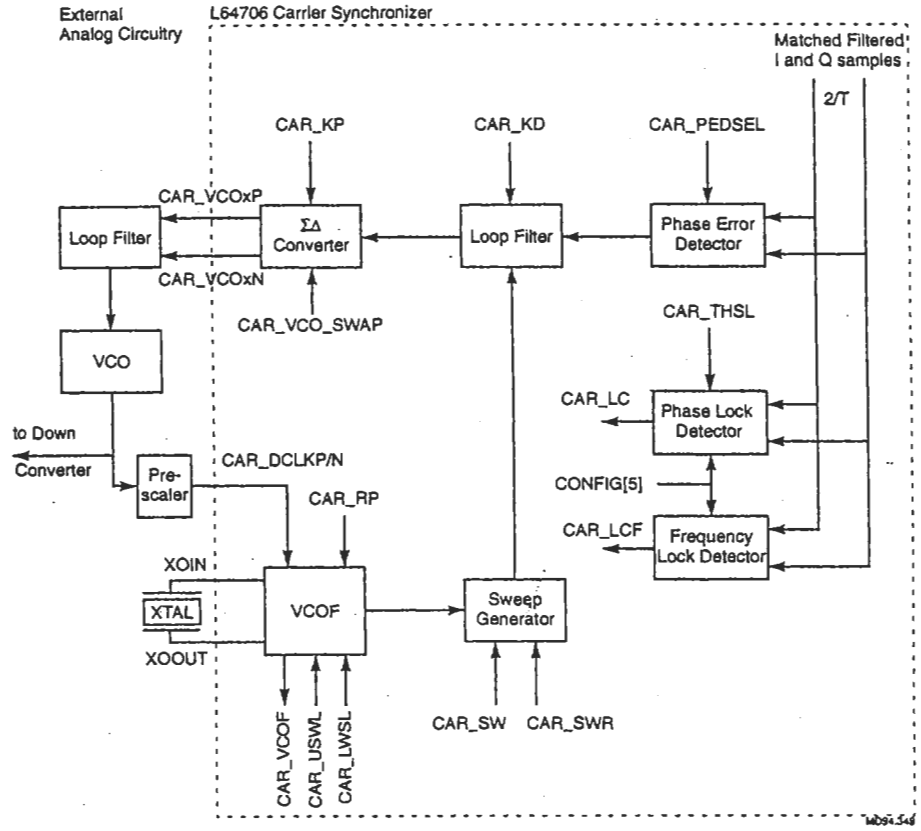
Clock

3.4 Carrier Synchronizer

Figure 3.2 illustrates the Carrier Synchronizer, which consists of the following functional elements:

- a phase error detector
- a digital loop filter
- a phase lock detector
- a frequency sweep generator
- a frequency lock detector

Figure 3.2
Carrier Recovery Loop



Because the outputs of off-the-shelf tuners for DVB satellite receivers have a large frequency uncertainty (a common order of magnitude is ±5 MHz), the L64706's Carrier Synchronizer includes a frequency sweep generator for signal acquisition.

To minimize the complexity of external analog circuitry for the loop filter, the L64706 implements part of the loop filter digitally. The external part of the loop filter consists of only fixed components whose values system

designers can choose to cover a whole range of data rates. The Carrier Synchronizer provides its output to the analog filter through two Sigma Delta differential pairs (CAR_VCOxP and CAR_VCOxN, where x = 1 and 2). Depending on the value of the CONFIG[2] bit, the Carrier Synchronizer selects one pair and 3-states the other pair. Externally, an analog integrator adds the signals together, where signals of pair 2 are weighted with a different factor with respect to the signals of pair 1. To change the weighting factor, choose different values for R_{CAR1} and R_{CAR2}. This feature provides a means for adjusting the loop bandwidth over a larger range than would be possible with pure Sigma Delta modulation.

3.4.1 Carrier Acquisition

During carrier acquisition, the internal frequency sweep generator searches for the correct frequency. To vary the sweep rate, change the value in the CAR_SWR register; to start the sweep generator, set the CAR_SW bit to one.

3.4.1.1 Frequency Sweep Limits

The CAR_USWL and CAR_LSWL registers set the upper and lower limits, respectively, of the frequency sweep.

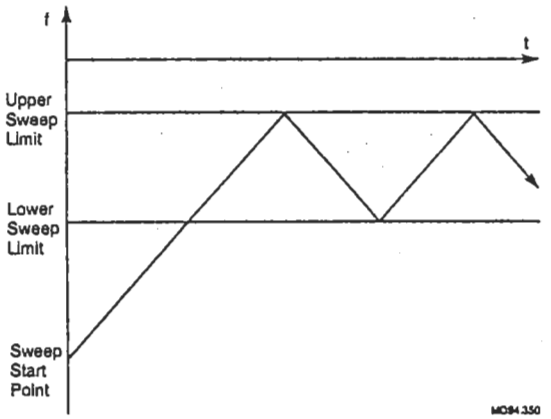
The frequency sweep uses an external crystal that produces a reference clock (same crystal as for clock acquisition). See Appendix A for details.

An external prescaler divides the frequency of the carrier VCO by a constant number (32, for example) and then feeds it to the L64706. The frequency from the prescaler should be larger than the crystal reference frequency and smaller than 80% of the CLK frequency.

The reference period for the VCO frequency measurement ends when a decrementing reference counter driven by the reference clock reaches zero. The L64706 loads the counter with the value in the 4-bit CAR_RP register, which defines the reference period in multiples of 1024 clock cycles.

The pre-scaled clock drives an incrementing counter, which the VCOF block resets at the beginning of and checks at the end of a reference period. If the pre-scaled frequency is below the lower limit set in the CAR_LWSL register, then the VCOF block automatically tells the sweep generator to increase the VCO frequency. If the pre-scaled frequency is above the upper limit set in the CAR_USWL register, then the VCOF block automatically tells the sweep generator to decrease the VCO frequency. Figure 3.3 illustrates how the sweep generator keeps the VCO frequency within the established limits.

Figure 3.3
Frequency
Sweeping



For example, consider the following frequency values:

- VCO nominal frequency = 480 MHz
- Frequency uncertainty = ±3 MHz
- Pre-scaling ratio = 32

With these values, the lower pre-scaled frequency is (480 – 3)/32 = 14.90625 MHz, and the upper pre-scaled frequency is (480 + 3)/32 = 15.09375 MHz.

If the CAR_RP register is set to 8, the reference period is 8192 reference clock cycles (for instance, at 10 MHz), and the upper and lower sweep limits must have the following values:

$$\text{CAR\_LSWL} = 14.90625 \times \frac{8192}{10} = 12,211 \text{ (lower limit)}$$

$$\text{CAR\_USWL} = 15.09375 \times \frac{8192}{10} = 12,365 \text{ (upper limit)}$$

3.4.1.2 Frequency Sweep Without Pre-scaled Frequency Signal

The frequency sweep generator can also operate without using the pre-scaled frequency—which can be very convenient if the analog front end does not provide for a prescaler function.

In this case, both the CAR_USWL and CAR_LSWL registers must be set to zero. The state of the CAR_SWEEP_SWP bit in the CAR_CONFIG register controls the sweep direction. Even though the Carrier Synchronizer controls the frequency sweep rate based on the value in the CAR_SWR register, the microprocessor must monitor the sweep direction itself.

3.4.1.3 Frequency Sweep Rate

The Carrier Synchronizer determines the frequency sweep rate based on the value in the CAR_SWR register. Set the value in the 8-bit CAR_SWR register based on Equation 3.7.

Equation 3.7

$$CAR\_SWR = 64 K_D \theta_\infty$$

K_D is the carrier phase error detector gain. Assuming a standard power reference value (the value in the PWR_REF register is 84), K_D has a typical value of 10 for low Eb/No conditions (4 dB) for both the DDML and the NDAML phase error detectors (see Section 3.4.3, "Carrier Phase Tracking"). For larger Eb/No conditions (10 dB), K_D is around 26 for the DDML and around 42 for the NDAML.

K_D grows linearly with $\sqrt{PWR\_REF}$. θ_∞ is the phase loop steady state error during acquisition. It should be taken strictly lower than 5 degrees. During the tracking phase, the loop drives the residual steady state error to 0.

Equation 3.8 gives the sweep rate in Hertz/sec.

Equation 3.8

$$\dot{f} = CAR\_SWR \cdot \frac{5}{128\pi} \cdot \frac{K_{VCO}}{R_{CAR} C_{CAR} (CAR\_KP)}$$

For example, if $K_D = 10$ and $\theta_\infty = 3° \approx 0.052$ rad, then CAR_SWR = 33.

3.4.1.4 Phase Lock Detection

Once the VCO frequency is close enough to the frequency of the incoming wave, the signal lies in the pull-in range of the phase lock loop. When the loop is phase locked, the phase lock detector sets the CAR_LC bit to one. To stop the sweep, the microprocessor must then set the CAR_SW bit to zero.

The phase lock detector uses a internal threshold and an estimation period, which are programmable via the CAR_THSL register and the CONFIG[4] bit, respectively.

CONFIG[4] selects between a long and a short estimation period.

For operation at low Eb/No (less than 10 dB), the long period should be selected (CONFIG[4] = 0). A typical value of CAR_THSL is then 31.

For operation at higher Eb/No (10 dB or higher), the short period can be selected, which then provides for a faster lock detection. In this case, a typical value for CAR_THSL is 72.

3.4.1.5 Frequency Lock Detection

The frequency lock detector also has a configurable estimation period, selectable by the same parameter as for phase lock detection (the CONFIG[4] bit).

No threshold values need be programmed here; the thresholds are fixed and hardcoded in the L64706.

3.4.1.6 False Locks

The microprocessor must take particular care to handle a false lock correctly. A false lock occurs when phase lock has been detected but the correct central frequency has not been reached yet. This situation happens in QPSK for frequency offsets that are multiples of 1/4T, where T is the QPSK symbol duration.

This case is detected by CAR_LC = 1 and CAR_LCF = 0. When the microprocessor detects this situation, it should set the CAR_OPEN bit to one and reset it after CAR_LC = 0. This has the effect of opening the carrier loop, forcing the loop to run out of the false lock point.

3.4.2 Carrier VCO Frequency Measurement

The L64706 puts the result of the VCO frequency measurement into the 16-bit CAR_VCOF register, which the microprocessor can read. Both nibbles must be read before the L64706 releases this register for a new value.

3.4.3 Carrier Phase Tracking

3.4.3.1 Phase Error Estimator

In QPSK mode (CONFIG[6] =0), the phase error detector implements two error estimators:

The phase error detector implements two error estimators:

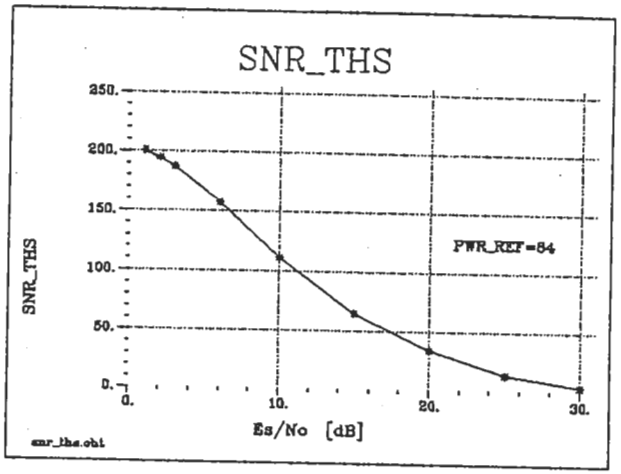
- a Non-data Aided Maximum Likelihood (NDAML) estimator
- a Decision Directed Maximum Likelihood (DDML) estimator

The microprocessor selects the estimator via the CAR_PED_SEL bit (bit 2 of the CAR_CONFIG register). CAR_PED_SEL = 0 sets the DDML estimator; CAR_PED_SEL = 1 sets the NDAML estimator.

In BPSK mode (CONFIG[6] = 1), the phase error detector inplements a single DDML estimator.

The phase detector uses two gain values depending on the signal to noise ratio. The SNR is internally estimated and compared to a threshold (parameter SNR_THS[7:0], address 11). The plot in Figure 3.4 shows the relation between the SNR_THS parameter and the actual Es/No on line (symbol energy to noise power density). The value SNR_THS = 100 corresponding to an actual Es/No = 11 dB is recommended. The result of the comparison of the estimated SNR to the threshold is stored in the STATUS[4] register (address 31).

Figure 3.4
SNR Threshold vs. ES/No



3.4.3.2 Loop Characteristics

To set the parameters of the carrier recovery loop (natural frequency, damping factor), system designers select the values the microprocessor writes into the CAR_KD and CAR_KP registers and the values of the resistors and capacitors of the external active filter.

The natural frequency ω_n (rad/s) and the damping factor ζ of the loop are determined by the following equations and illustrated in Section 4.2, "Input Waveforms."

Equation 3.9

$$\zeta = 2 \cdot \text{CAR\_KD} \cdot \omega_n \cdot T, \qquad \omega_n = \sqrt{\frac{5 K_D K_{CARVCO}}{R_{CAR} C_{CAR} (\text{CAR\_KP})}}$$

T represents the QPSK symbol duration. Twice the value of the CAR_KP parameter determines the resolution of the Sigma Delta conversion; it should be kept above 30 for 6 bits of resolution.

The loop filter output is provided with a Sigma Delta modulated complementary signal pair, CAR_VCOxP and CAR_VCOxN (x = 1 or 2), to the external active integrator, which completes the loop filter chain. Depending on the CAR_CONFIG[4:5] bit settings, the complementary pairs are

selected or 3-stated. After reset, both complementary pairs are active. Externally, these signals are added together in the analog integrator, where the CAR_VCO2P/N outputs should be weighted with a different factor with respect to the CAR_VCO1P/N outputs by proper selection of the corresponding resistors and capacitors. This selection provides a means for adjusting the loop bandwidth over a large range of data rates.

For a carrier loop with a VCO gain K_{CARVCO}, Equations 3.10 and 3.11 provide the recommended R and C values shown in Figure 4.5 on page 4-7.

Equation 3.10

$$R_{CAR1}C_{CAR} = \frac{K_{CARVCO}}{3.98\times10^{8}} \text{ sec}$$

Equation 3.11

$$R_{CAR2}C_{CAR} = \frac{K_{CARVCO}}{7.22\times10^{8}} \text{ sec}$$

Use R_{CAR1} and C_{CAR} for operation in the range from 12 to 30 Mbaud, and R_{CAR2} and C_{CAR} in the range from 5 to 12 Mbaud.

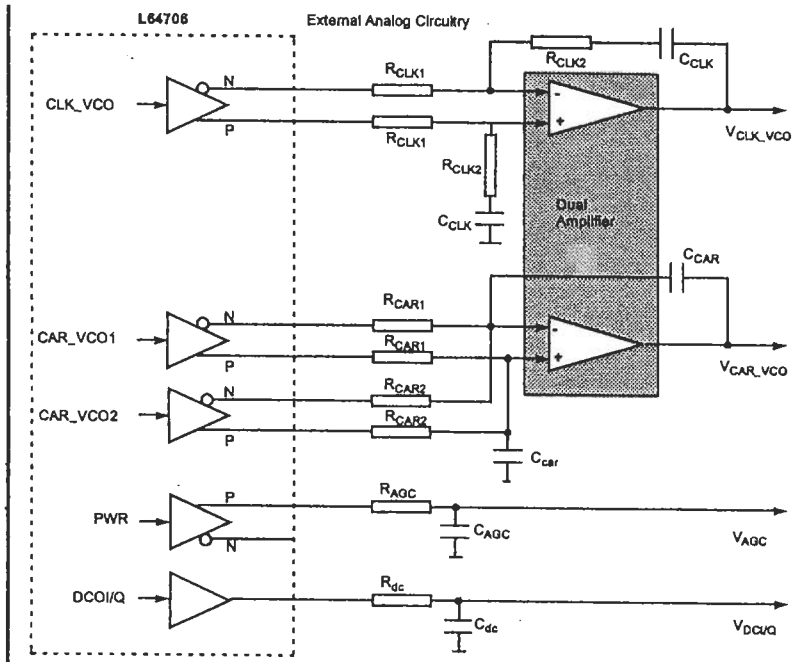
3.4.3.3 Low Baud Rate Operation

For low baud rate operation (between 1 and 5 Mbaud), the Sigma-Delta conversion used in the carrier loop introduces a delay that makes the carrier loop too narrow for reliable operation.

For this type of application, use the CAR_PED[5:0] signal instead of the CAR_VCOxP/N outputs. The CAR_PED signal is simply the digitalk signal before Sigma-Delta conversion. It is intended to be connected to an external 6-bit DAC, which then feeds the same active low-pass filter as described before.

The external DAC may use the DATA_VALID signal as a clock.

Figure 4.5
Loop Control Signals Interface



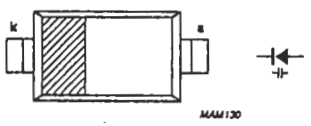
VHF variable capacitance diode BB133

FEATURES

- Excellent linearity
- Excellent matching to 0.7% DMA
- Very small plastic SMD package
- C28: 2.5 pF; ratio: 16
- Low series resistance.

APPLICATIONS

- Electronic tuning in VHF television tuners, band B up to 460 MHz
- VCO.



Marking code: P3.
Cathode side indicated by a bar.

Fig.1 Simplified outline (SOD323) and symbol.

DESCRIPTION

The BB133 is a variable capacitance diode, fabricated in planar technology, and encapsulated in the SOD323 very small plastic SMD package.

The excellent matching performance is achieved by gliding matching and a direct matching assembly procedure. The unmatched type, BB150 has the same specification.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_R	continuous reverse voltage	–	30	V
I_F	continuous forward current	–	20	mA
T_{stg}	storage temperature	−55	+150	°C
T_j	operating junction temperature	−55	+125	°C

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

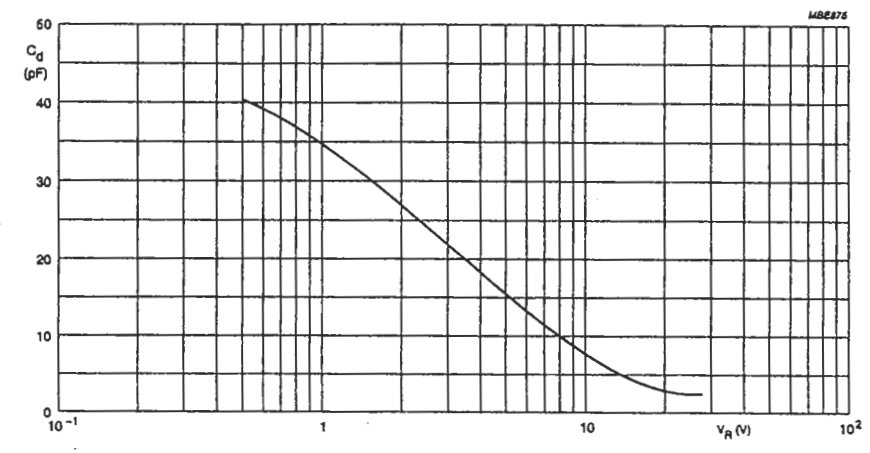
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_R	reverse current	V_R = 30 V; see Fig.3	–	10	nA
		V_R = 30 V; T_j = 85 °C; see Fig.3	–	200	nA
r_s	diode series resistance	f = 100 MHz; note 1	–	0.9	Ω
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz; see Figs 2 and 4	38	46	pF
		V_R = 28 V; f = 1 MHz; see Figs 2 and 4	2.2	2.6	pF
$\frac{C_{d(0.5V)}}{C_{d(28V)}}$	capacitance ratio	f = 1 MHz	14	21	
$\frac{\Delta C_d}{C_d}$	capacitance matching	V_R = 0.5 to 28 V; in a sequence of 4 diodes (gliding)	–	0.7	%
		V_R = 0.5 to 28 V; in a sequence of 15 diodes (gliding)	–	2	%

Note

1. V_R is the value at which C_d = 30 pF.

VHF variable capacitance diode BB133

GRAPHICAL DATA



f = 1 MHz; T_j = 25 °C.

Fig.2 Diode capacitance as a function of reverse voltage; typical values.

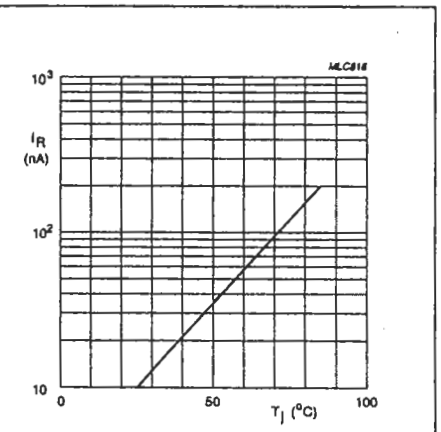
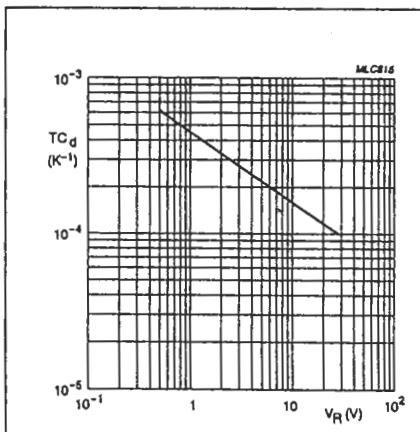


Fig.3 Reverse current as a function of junction temperature; maximum values.



T_j = 0 to 85 °C.

Fig.4 Temperature coefficient of diode capacitance as a function of reverse voltage; typical values.

National Semiconductor

January 2003

LM833
Dual Audio Operational Amplifier

General Description

The LM833 is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

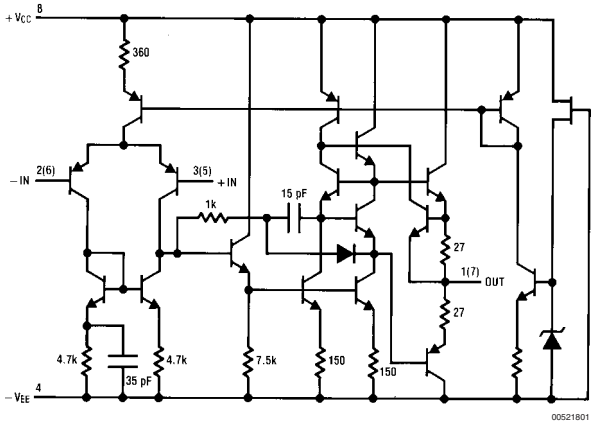
This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833 is pin-for-pin compatible with industry standard dual operational amplifiers.

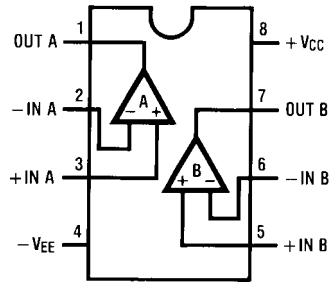
Features

- Wide dynamic range: >140dB
- Low input noise voltage: 4.5nV/√Hz
- High slew rate: 7 V/µs (typ); 5V/µs (min)
- High gain bandwidth: 15MHz (typ); 10MHz (min)
- Wide power bandwidth: 120KHz
- Low distortion: 0.002%
- Low offset voltage: 0.3mV
- Large phase margin: 60˚
- Available in 8 pin MSOP package

Schematic Diagram (1/2 LM833)



Connection Diagram



Order Number LM833M, LM833MX, LM833N, LM833MM or LM833MMX
See NS Package Number
M08A, N08E or MUA08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage $V_{CC}-V_{EE}$	36V
Differential Input Voltage (Note 3) V_I	±30V
Input Voltage Range (Note 3) V_{IC}	±15V
Power Dissipation (Note 4) P_D	500 mW
Operating Temperature Range T_{OPR}	−40 ~ 85˚C
Storage Temperature Range T_{STG}	−60 ~ 150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260˚C
Small Outline Package (SOIC and MSOP)	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C
ESD tolerance (Note 5)	1600V

DC Electrical Characteristics (Notes 1, 2)

(T_A = 25˚C, V_S = ±15V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	R_L = 2 kΩ, V_O = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 10 kΩ	±12	±13.5		V
		R_L = 2 kΩ	±10	±13.4		V
V_{CM}	Input Common-Mode Range		±12	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15~5V, −15~−5V	80	100		dB
I_Q	Supply Current	V_O = 0V, Both Amps		5	8	mA

AC Electrical Characteristics

(T_A = 25˚C, V_S = ±15V, R_L = 2 kΩ)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	R_L = 2 kΩ	5	7		V/µs
GBW	Gain Bandwidth Product	f = 100 kHz	10	15		MHz

Design Electrical Characteristics

(T_A = 25˚C, V_S = ±15V) The following parameters are not tested or guaranteed.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	µV/˚C
THD	Distortion	R_L = 2 kΩ, f = 20~20 kHz V_{OUT} = 3 Vrms, A_V = 1	0.002	%
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1 kHz	4.5	$nV/\sqrt{Hz}$
i_n	Input Referred Noise Current	f = 1 kHz	0.7	$pA/\sqrt{Hz}$
PBW	Power Bandwidth	V_O = 27 V_{pp}, R_L = 2 kΩ, THD ≤ 1%	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
ϕ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	f = 20~20 kHz	−120	dB

Design Electrical Characteristics (Continued)

Note 1: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: All voltages are measured with respect to the ground pin, unless otherwise specified.

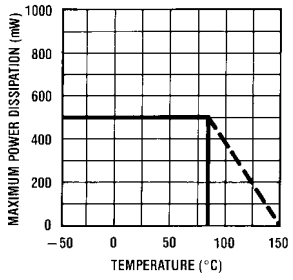
Note 3: If supply voltage is less than ±15V, it is equal to supply voltage.

Note 4: This is the permissible value at $T_A \leq 85˚C$.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

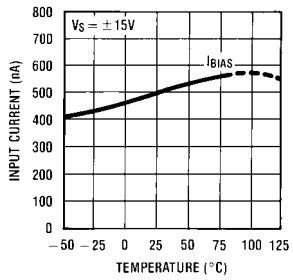
Typical Performance Characteristics

Maximum Power Dissipation vs Ambient Temperature



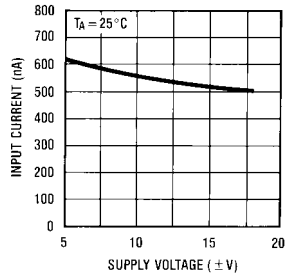
00521804

Input Bias Current vs Ambient Temperature



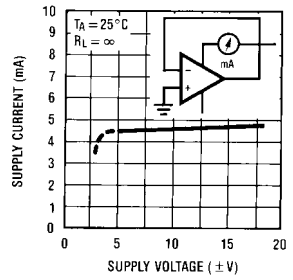
00521805

Input Bias Current vs Supply Voltage



00521806

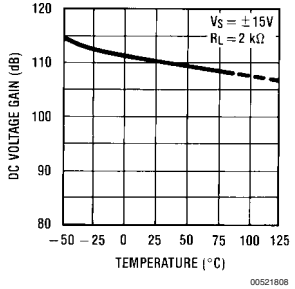
Supply Current vs Supply Voltage



00521807

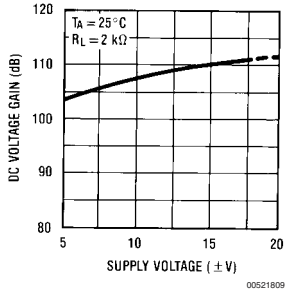
Typical Performance Characteristics (Continued)

DC Voltage Gain vs Ambient Temperature



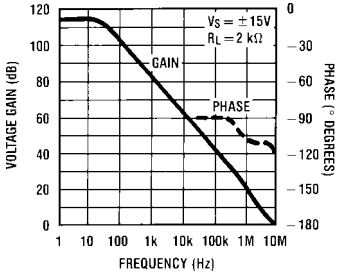
00521808

DC Voltage Gain vs Supply Voltage



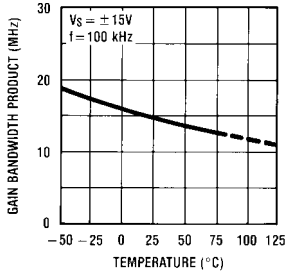
00521809

Voltage Gain & Phase vs Frequency



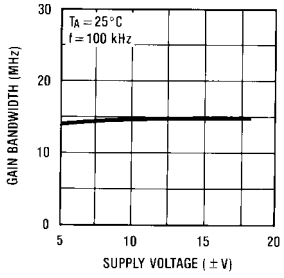
00521810

Gain Bandwidth Product vs Ambient Temperature



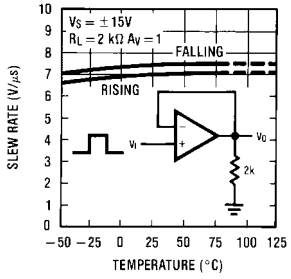
00521811

Gain Bandwidth vs Supply Voltage



00521812

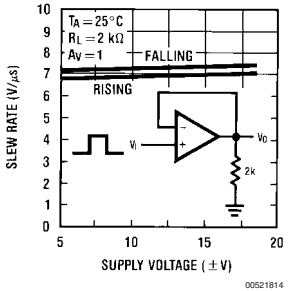
Slew Rate vs Ambient Temperature



00521813

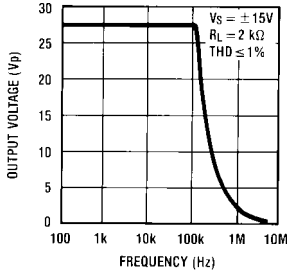
Typical Performance Characteristics (Continued)

Slew Rate vs Supply Voltage



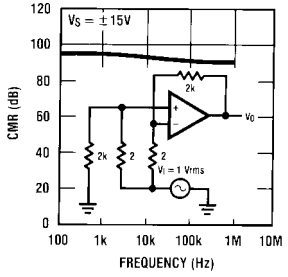
00521814

Power Bandwidth



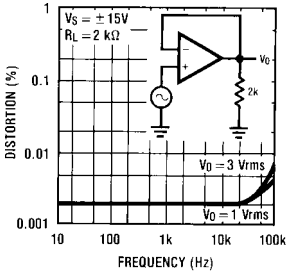
00521815

CMR vs Frequency



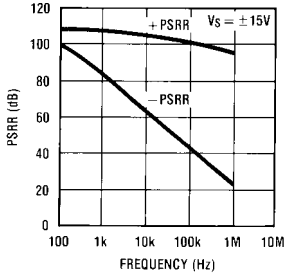
00521819

Distortion vs Frequency



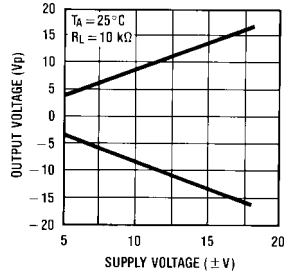
00521820

PSRR vs Frequency



00521818

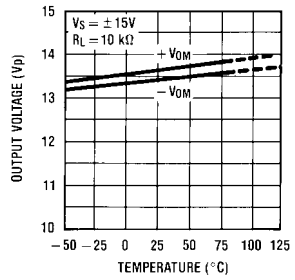
Maximum Output Voltage vs Supply Voltage



00521816

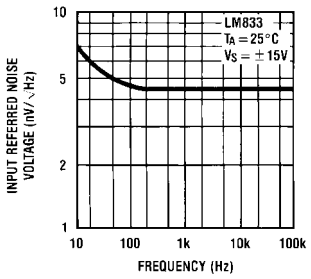
Typical Performance Characteristics (Continued)

Maximum Output Voltage vs Ambient Temperature



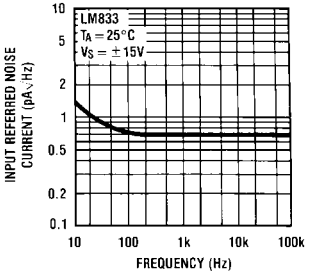
00521817

Spot Noise Voltage vs Frequency



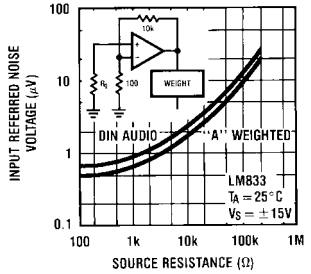
00521821

Spot Noise Current vs Frequency



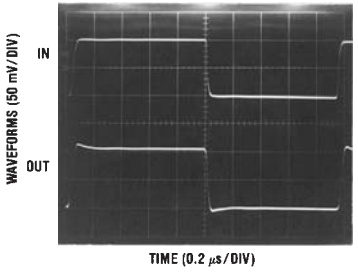
00521822

Input Referred Noise Voltage vs Source Resistance



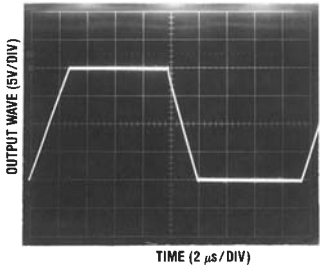
00521823

Noninverting Amp



00521824

Noninverting Amp



00521825

FEATURES

- Access time : 35/70ns (max.)
- Low power consumption :
  Operating : 200 mW (typical)
  Standby : 2.5mW (typical) Normal
  50µW (typical) L-version
  5µW (typical) LL-version
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 32-pin 600 mil PDIP
  32-pin 450 mil SOP
  32-pin 8x20mm TSOP-1

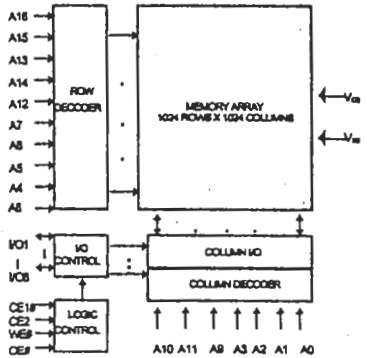
GENERAL DESCRIPTION

The UT621024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

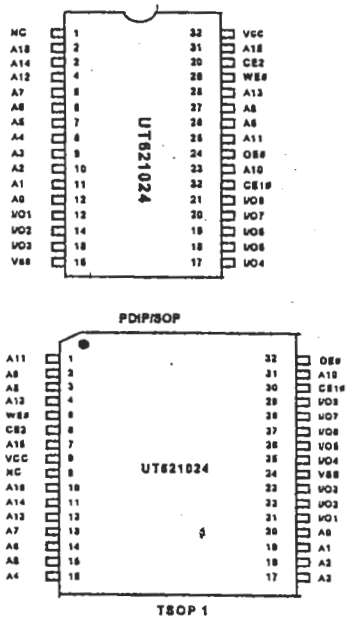
The UT621024 is designed for low power application. It is particularly well suited for battery back-up nonvolatile memory application.

The UT621024 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1#, CE2	Chip Enable 1,2 Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

UTRON

UT621024

Rev. 1.2

128K X 8 BIT LOW POWER CMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.5 to +7.0	V
Operating Temperature	T_A	0 to +70	℃
Temperature Under Bias	T_{BIAS}	-55 to +125	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_T	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE1#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1}
Standby	X	L	X	X	High -Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V± 10%, TA = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}			2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{SS} \leq V_{I/O} \leq V_{CC}$		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = - 1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA		-	-	0.4	V
DC Operating Power	I_{CC}	CE1# = V_{IL}, CE2=V_{IH}		-	7	15	mA
Average Operating	I_{CC1}	Cycle time = 1µs, 100% Dut		-	-	10	mA
	I_{CC2}	Min.Cycle, 100% Duty, CE1# =V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0mA	- 35	-	60	100	mA
			- 70	-	40	70	mA
Standby Power	I_{SB}	CE1# =V_{IH} or CE2 = V_{IL}	Norma	-	-	10	mA
			-L	-	-	3	mA
			-LL				
Supply Current	I_{SB1}	CE1# ≧ V_{CC}-0.2V or	Norma	-	0.5	5	mA
			- L	-	10	300*	µA
		CE2 ≦ 0.2V	- LL	-	1	15*	µA

*Those parameters are guaranteed by temperature range from 0℃ to 50℃

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=100pF, I_{OH}/I_{OL}=-1mA/4mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V± 10% , T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT621024-35		UT621024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	70	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE2}	-	35	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ1}*, t_{CLZ2}*	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ1}*, t_{CHZ2}*	-	25	-	35	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

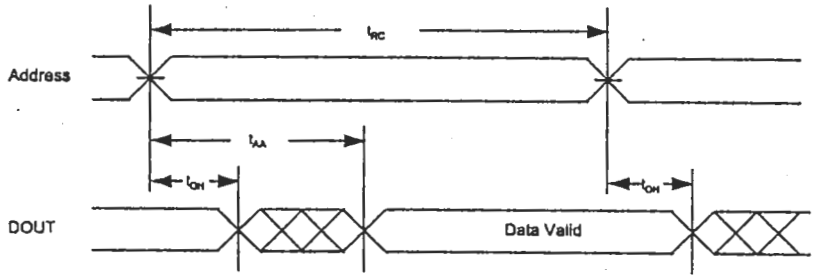
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT621024-35		UT621024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	60	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	30	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	45	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	25	ns

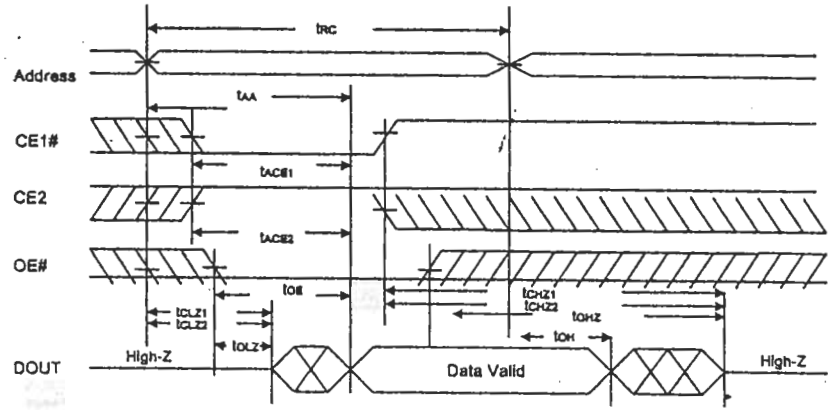
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)

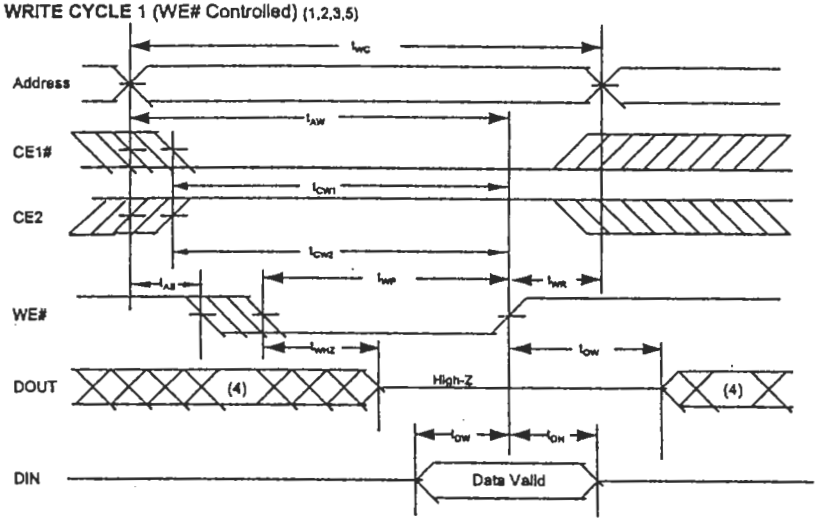


READ CYCLE 2 (CE1#, CE2 and OE# Controlled) (1,3,5,6)

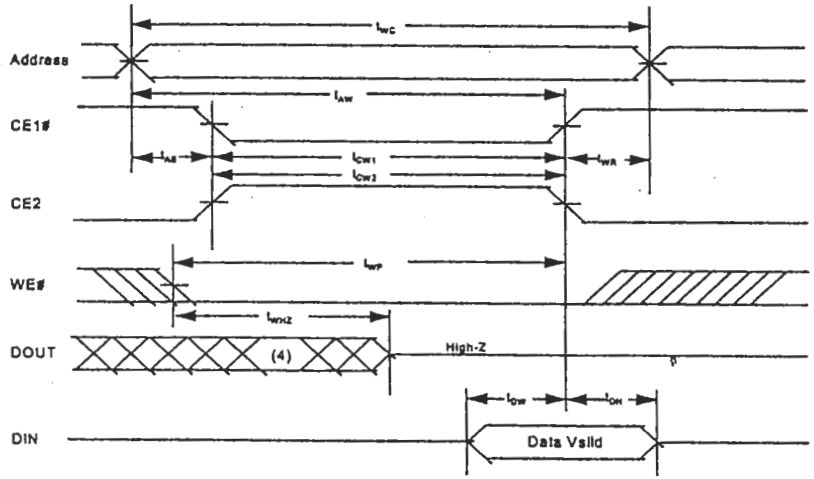


Notes :
1. WE# is HIGH for read cycle.
2. Device is continuously selected CE1#=V_{IL} and CE2=V_{IH}.
3. Address must be valid prior to or coincident with CE1# and CE2 transition; otherwise t_{AA} is the limiting parameter.
4. OE# is low.
5. t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1}, t_{CHZ2} is less than t_{CLZ2}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)



WRITE CYCLE 2 (CE1# and CE2 Controlled) (1,2,5)



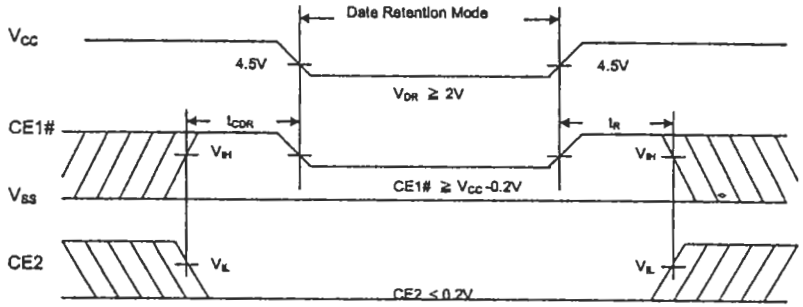
Notes :
1. WE# or CE1# must be HIGH or CE2 must be LOW during all address transitions.
2. A write occurs during the overlap of a low CE1#, a high CE2 and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the CE1# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.

DATA RETENTION CHARACTERISTICS (T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	CE1# ≧ Vcc-0.2V or CE2 ≤ 0.2V		2.0	-	-	V
Data Retention Current	I_{DR}	Vcc=3V	- L	-	1	50	µA
		CE1# ≧ Vcc-0.2V or CE2 ≤ 0.2V	- LL	-	0.5	20	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC}*	-	-	ns

t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

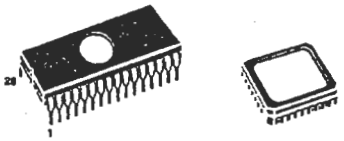


SGS-THOMSON MICROELECTRONICS

M27C4001

4 Megabit (512K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)



FDIP32W (F)

LCCC32W (L)

PLCC32 (C)

TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27C4001 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 524,288 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

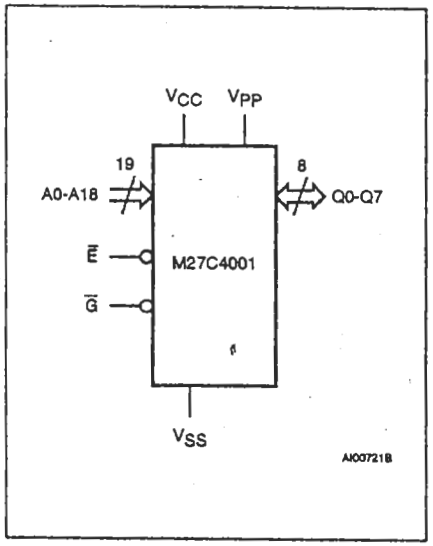


Figure 2A. DIP Pin Connections

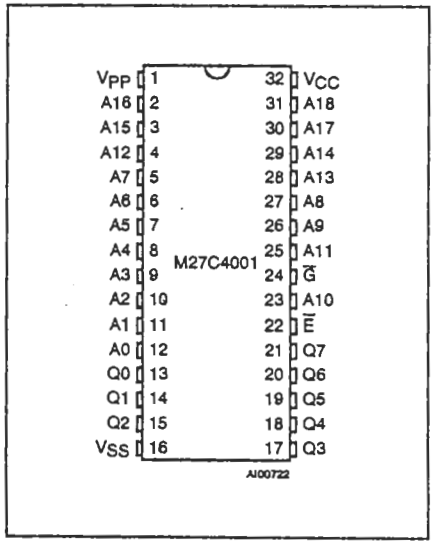


Figure 2B. LCC Pin Connections

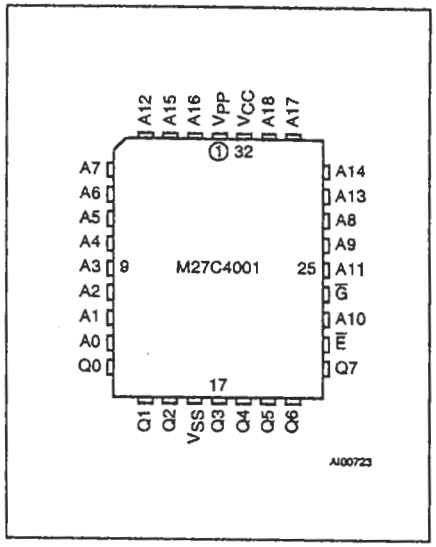
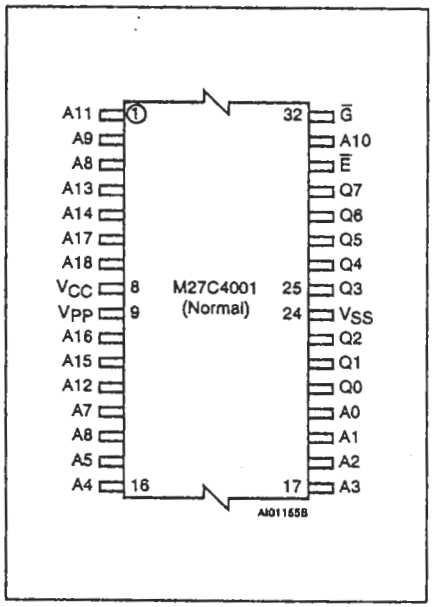


Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C4001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C4001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C4001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

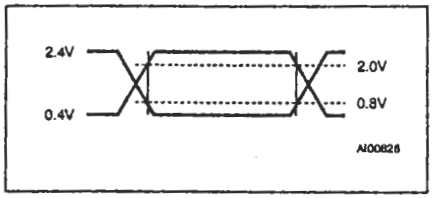


Figure 4. AC Testing Load Circuit

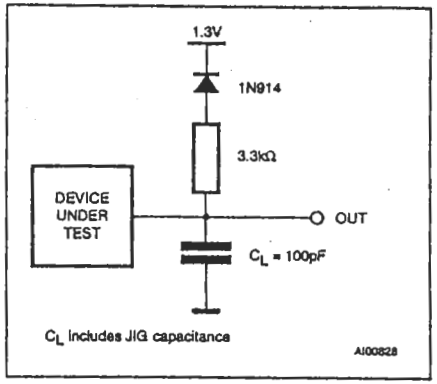


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

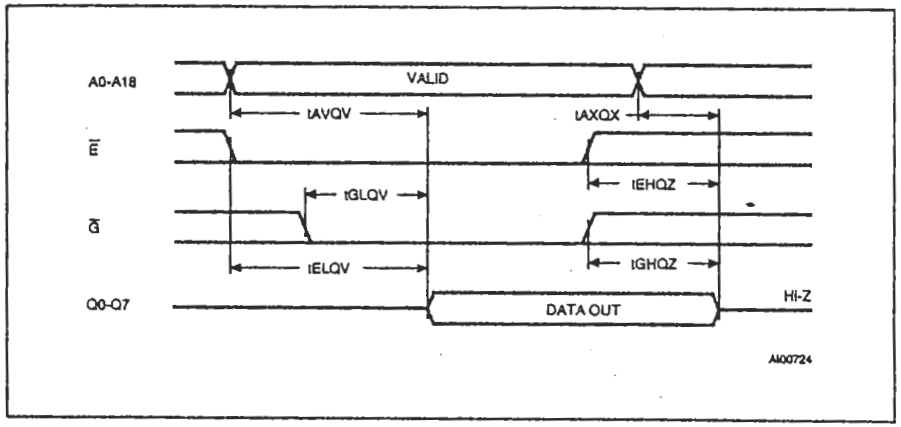


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4001						Unit
				-70		-80		-90		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4001						Unit
				-10		-12		-15		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0 ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E}$ = V_{IL}		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

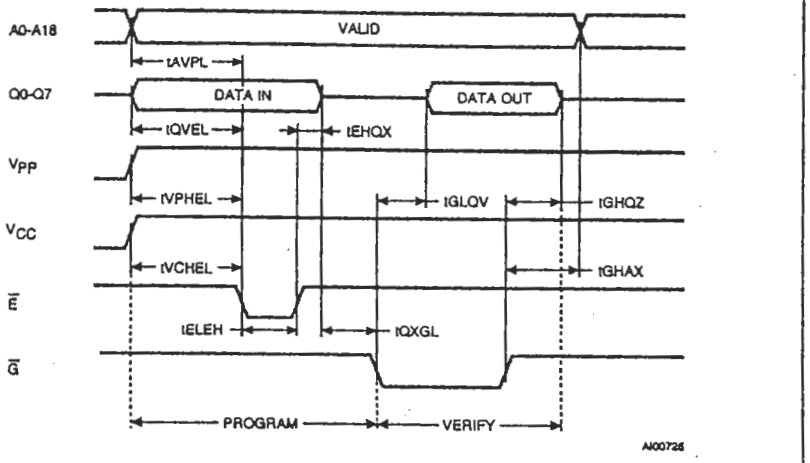
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



System Considerations

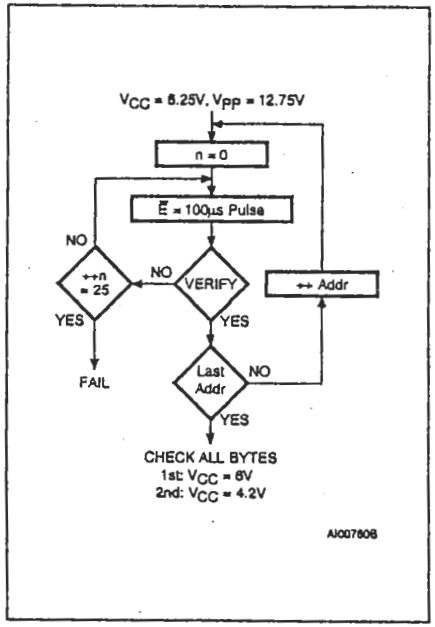
The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C4001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C4001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C4001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C4001 may be common. A TTL low level pulse applied to a M27C4001's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C4001. A high level $\overline{E}$ input inhibits the other M27C4001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4001 with $V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C4001, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C4001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C4001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C4001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

FINAL

Am29F010

1 Megabit (128 K x 8-bit)
CMOS 5.0 Volt-only, Uniform Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — 5.0 V ± 10% for read, erase, and program operations
  - — Simplifies system-level power requirements
- **High performance**
  - — 45 ns maximum access time
- **Low power consumption**
  - — 30 mA max active read current
  - — 50 mA max program/erase current
  - — <25 µA typical standby current
- **Flexible sector architecture**
  - — Eight uniform sectors
  - — Any combination of sectors can be erased
  - — Supports full chip erase
- **Sector protection**
  - — Hardware-based feature that disables/re-enables program and erase operations in any combination of sectors
  - — Sector protection/unprotection can be implemented using standard PROM programming equipment
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically pre-programs and erases the chip or any combination of designated sector
  - — Embedded Program algorithm automatically programs and verifies data at specified address
- **Minimum 100,000 program/erase cycles guaranteed**
- **Package options**
  - — 32-pin PLCC
  - — 32-pin TSOP
  - — 32-pin PDIP
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash
  - — Superior inadvertent write protection
- **Data# Polling and Toggle Bits**
  - — Provides a software method of detecting program or erase cycle completion

Publication# 16736 Rev: G Amendment/+3
Issue Date: July 1998

GENERAL DESCRIPTION

The Am29F010 is a 1 Mbit, 5.0 Volt-only Flash memory organized as 131,072 bytes. The Am29F010 is offered in 32-pin PLCC, TSOP, and PDIP packages. The byte-wide data appears on DQ0-DQ7. The device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations. The device can also be programmed or erased in standard EPROM programmers.

The standard device offers access times of 45, 55, 70, 90, and 120 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This invokes the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This invokes the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is erased when shipped from the factory.

The **hardware data protection** measures include a low V_{CC} detector automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory, and is implemented using standard EPROM programmers.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

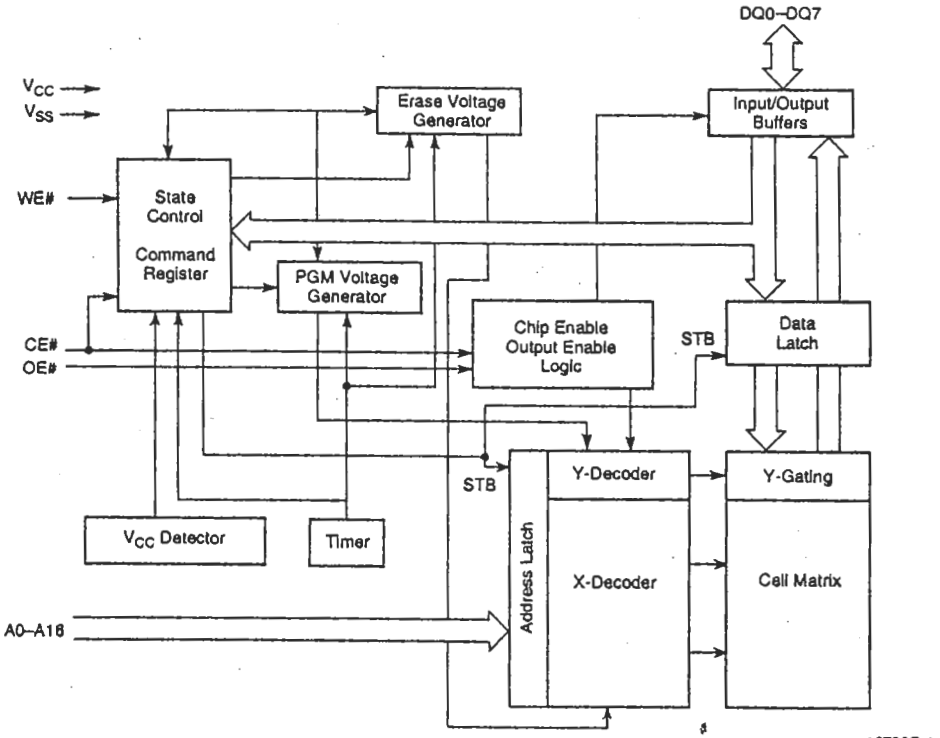
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

PRODUCT SELECTOR GUIDE

Family Part Number		Am29F010				
Speed Option	V_{CC} = 5.0 V ± 5%	-45	-55 (P)			
	V_{CC} = 5.0 V ± 10%		-55 (J, E, F)	-70	-90	-120
Max Access Time (ns)		45	55	70	90	120
CE# Access (ns)		45	55	70	90	120
OE# Access (ns)		25	30	30	35	50

Note: See the AC Characteristics section for full specifications.

BLOCK DIAGRAM



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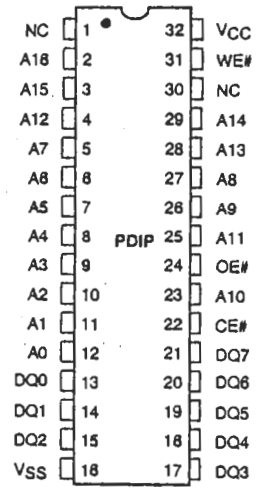
CONNECTION DIAGRAMS



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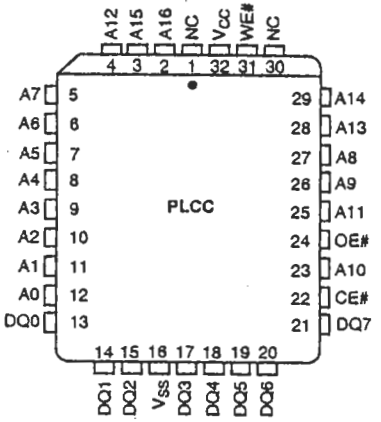
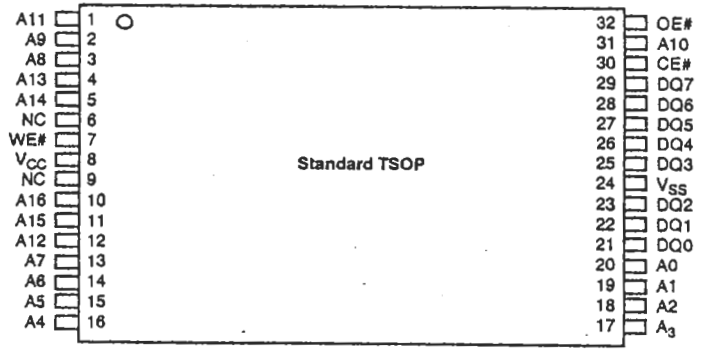


16736G-3



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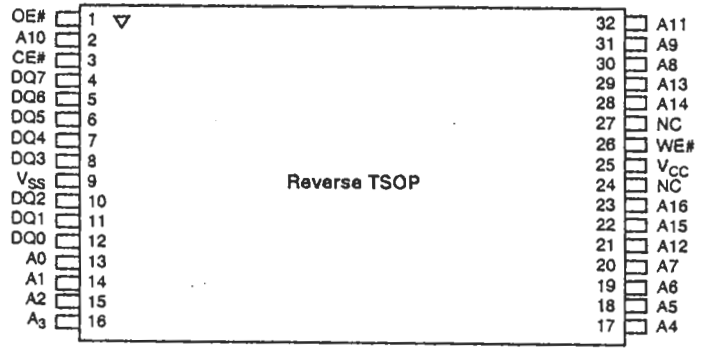


16736G-5

PIN CONFIGURATION

A0–A16 = 17 Addresses

DQ0–DQ7 = 8 Data Inputs/Outputs

CE# = Chip Enable

OE# = Output Enable

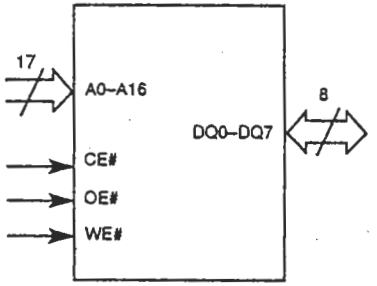
WE# = Write Enable

V_{CC} = +5.0 Volt Single Power Supply
(See Product Selector Guide for speed options and voltage supply tolerances)

V_{SS} = Device Ground

NC = Pin Not Connected Internally

LOGIC SYMBOL



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DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29F010 Device Bus Operations

Operation	CE#	OE#	WE#	Addresses (Note 1)	DQ0–DQ7
Read	L	L	H	A_{IN}	D_{OUT}
Write	L	H	L	A_{IN}	D_{IN}
Standby	$V_{CC} \pm 0.5$ V	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z
Hardware Reset	X	X	X	X	High-Z
Temporary Sector Unprotect	X	X	X	A_{IN}	D_{IN}

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Addresses In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. *Addresses are A16:A0.*
2. *The sector protect and sector unprotect functions must be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section in the appropriate data sheet for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# pin is held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when CE# is held at V_{IH}. The device requires the standard access time (t_{CE}) before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics tables represents the standby current specification.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29F010 Sector Addresses Table

Sector	A16	A15	A14	Address Range
SA0	0	0	0	00000h-03FFFh
SA1	0	0	1	04000h-07FFFh
SA2	0	1	0	08000h-0BFFFh
SA3	0	1	1	0C000h-0FFFFh
SA4	1	0	0	10000h-13FFFh
SA5	1	0	1	14000h-17FFFh
SA6	1	1	0	18000h-1BFFFh
SA7	1	1	1	1C000h-1FFFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 3. Am29F010 Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A16 to A14	A13 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29F010	L	L	H	X	X	V_{ID}	X	L	X	L	H	20h
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h (protected)
												00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. Details on this method are provided in a supplement, publication number 20495. Contact an AMD representative to obtain a copy of the appropriate document.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

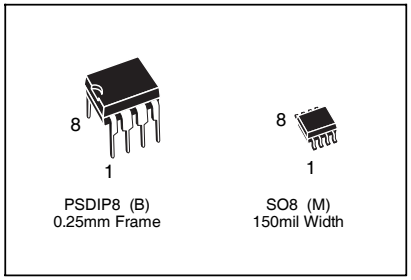
Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

ST24C16, ST25C16
ST24W16, ST25W16

16 Kbit Serial I^2C Bus EEPROM with User-Defined Block Write Protection

- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES) for the ST24C16
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



DESCRIPTION

This specification covers a range of 16 Kbit I^2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.

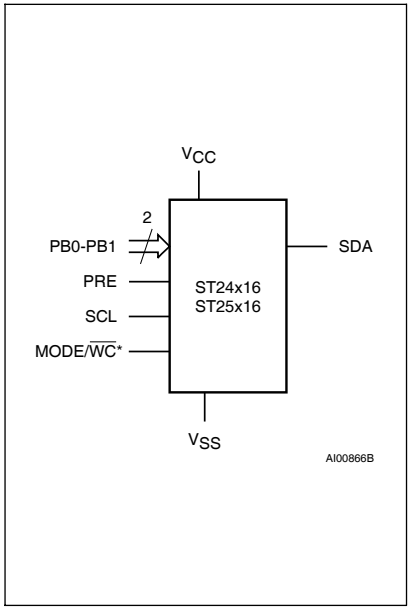
The ST24/25x16 are 16 Kbit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x8 bits. These are manufactured in STMicroelectronics's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memories behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the

Table 1. Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W16 products.

Figure 2A. DIP Pin Connections

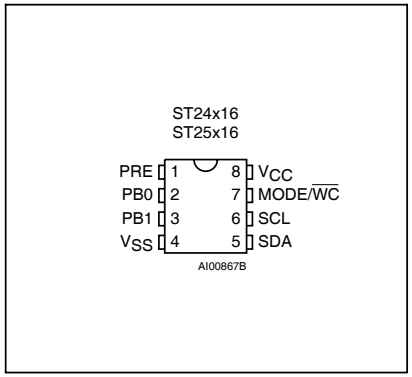


Figure 2B. SO8 Pin Connections

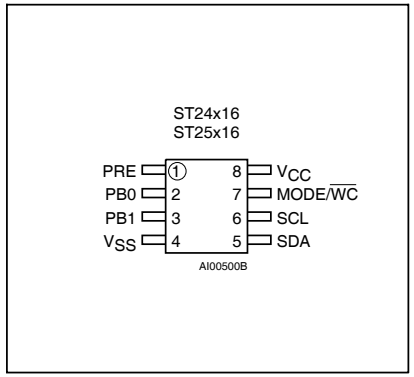


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Table 3. Device Select Code

	Device Code				Memory MSB Addresses			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	A10	A9	A8	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	MODE pin	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'			reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 2048	As CURRENT or RANDOM Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write	'0'	V_{IH}	8	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, RW = '0'

Note: X = V_{IH} or V_{IL}.

memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the 4 upper blocks of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. The block in which the protection starts is selected by the input pins PB0, PB1. Protection is enabled by setting a Protect Flag bit when the PRE input pin is driven High.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input signal is used to synchronise all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA signal is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Protected Block Select (PB0, PB1). PB0 and PB1 input signals select the block in the upper part of the memory where write protection starts. These inputs have a CMOS compatible input level.

Protect Enable (PRE). The PRE input signal, in addition to the status of the Block Address Pointer bit (b2, location 7FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also WC feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control (WC). An hardware Write Control feature is offered only for ST24W16 and ST25W16 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC at V_{IH}) or disable (WC at V_{IL}) the internal write protection. When unconnected, the WC input is internally read as V_{IL}. The devices with this Write Control feature no longer supports the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

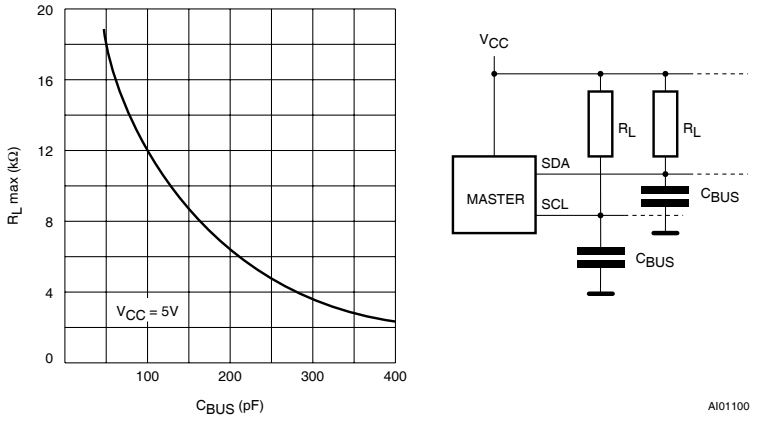


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W16)	$V_{IN} \le 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W16)	$V_{IN} \ge 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (PB0 - PB1, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (PB0 - PB1, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

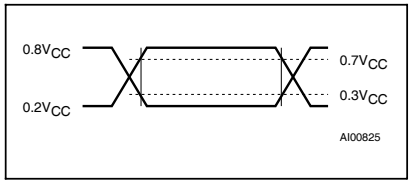
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W (3)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.
3. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (5 address MSB are not constant) the maximum programming time is doubled to 20ms.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION

I²C Bus Background

The ST24/25x16 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x16 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x16 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Figure 5. AC Waveforms

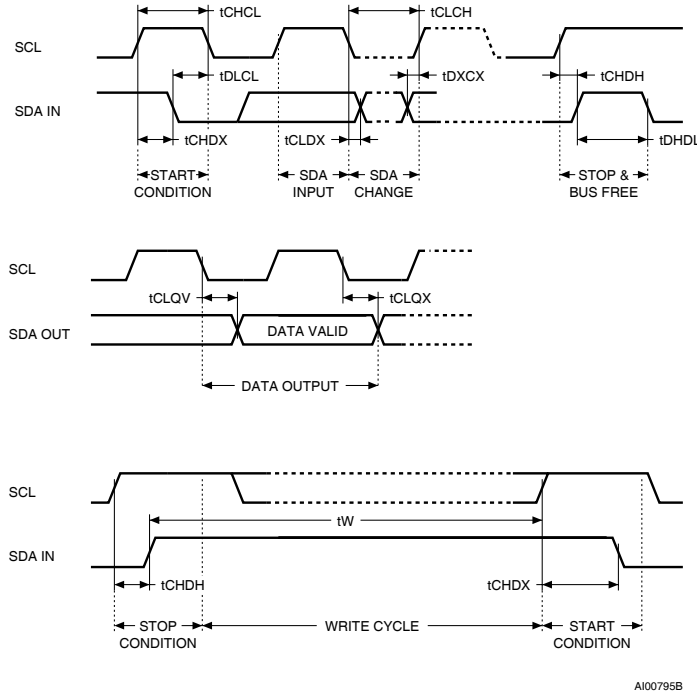
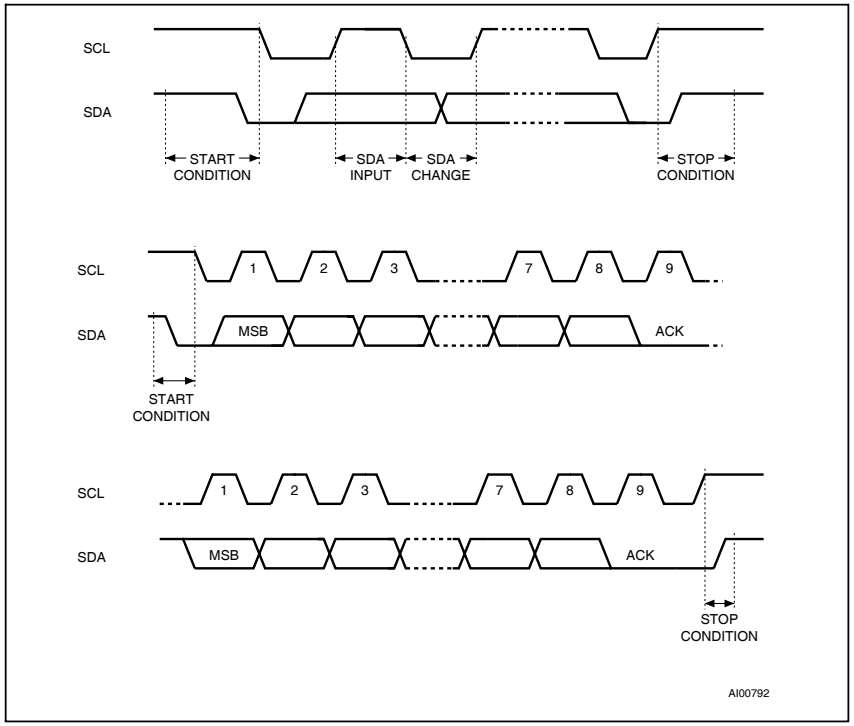


Figure 6. I²C Bus Protocol



Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x16 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

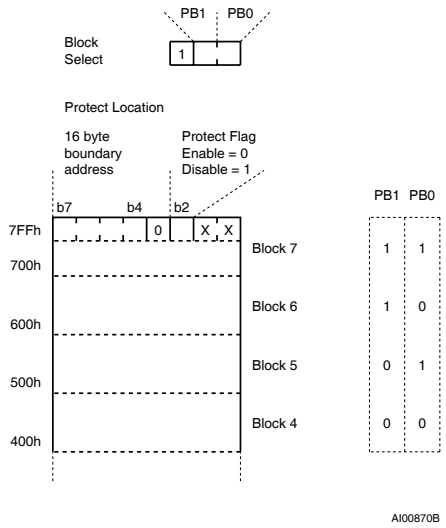
Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x16 samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x16, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifie the device type (1010), 3 Block select bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. They are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Figure 7. Memory Protection



Write Operations

The Multibyte Write mode (only available on the ST24/25C16 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes of one memory block. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W16 versions, any write command with $\overline{WC}$ = '1' (during a period of time from the START condition untill the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 10.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write (ST24/25C16 only). For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 contiguous rows (one row is 16 bytes), the programming time is then doubled to a maximum of 20ms. Writing more than 8 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 16 bytes long). However, the Multibyte Write can properly write up to 16 consecutive bytes only if the first address of these 16 bytes is the first address of the row, the 15 following bytes being written in the 15 following bytes of this same row.

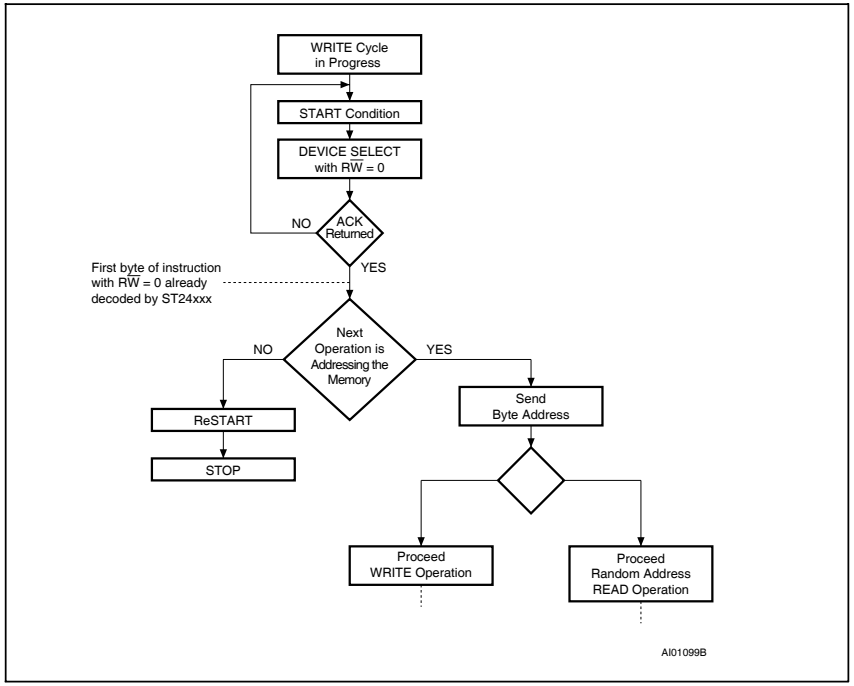
Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the same Block Address bits (b3, b2, b1 of Device Select code in Table 3) and the same 4 MSBs in the Byte Address. The master sends one up to 16 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

– Initial condition: a Write is in progress (see Figure 8).
– Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
– Step 2: if the memory is internally writing, no ACK will be returned. The Master goes back to Step1. If the memory has terminated the internal writing, it will issue an ACK indicating that the memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step 1).

Figure 8. Write Cycle Polling using ACK



Write Protection. Data in the upper four blocks of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 7FFh).The boundary address is user defined by writing it in the Block Address Pointer (location 7FFh).

The Block Address Pointer is an 8 bit EEPROM register located at the address 7FFh. It is composed by 4 MSBs Address Pointer, which defines the bottom boundary address, and 4 LSBs which must be programmed at '0'. This Address Pointer can therefore address a boundary by page of 16 bytes.

The block in which the Block Address Pointer defines the boundary of the write protected memory is defined by the logic level applied on the PB1 and PB0 input pins:

– PB1 ='0'and PB0 ='0' select block 4
– PB1 ='0'and PB0 ='1' select block 5
– PB1 ='1'and PB0 ='0' select block 6
– PB1 ='1'and PB0 ='1' select block 7

The following sequence should be used to set the Write Protection:

– write the data to be protected into the top of the memory, up to, but not including, location 7FFh;
– select the block by hardwiring the signals PB0 & PB1;
– set the protection by writing the correct bottom boundary address in the Address Pointer (4 MSBs of location 7FFh) with bit b2 (Protect Flag) set to '0'.

Note that for a correct fonctionality of the memory, all the 4 LSBs of the Block Address Pointer must also be programmed at '0'. The area will be protected when the PRE input is taken High.

Remark: The Write Protection is active if and only if the PRE input pin is driven High and the bit 2 of location 7FFh is set to '0'. In all the other cases, the memory Block will not be protected. While the PRE input pin is read at '0' by the memory, the location 7FFh can be used as a normal EEPROM byte.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 7 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 7FFh, by 7 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 16 bytes lower boundary of the protected area.

Figure 9. Write Modes Sequence (ST24/25C16)

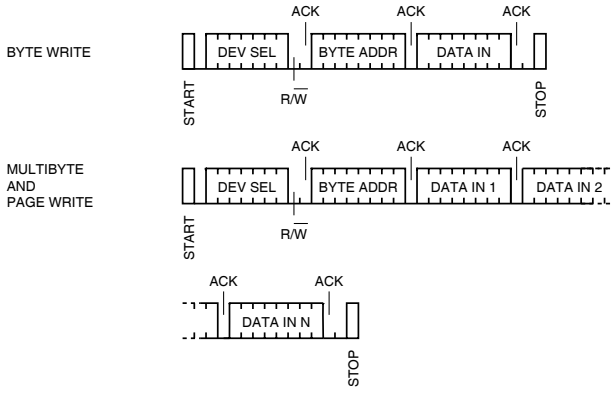
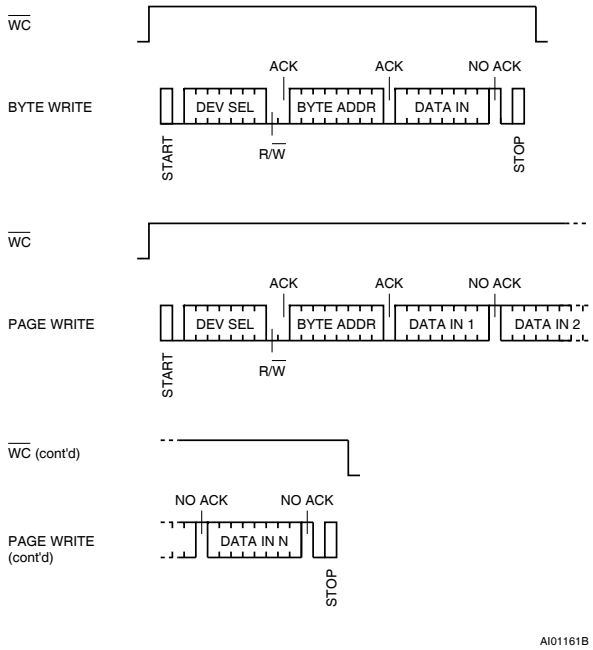


Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W16)



Read Operation

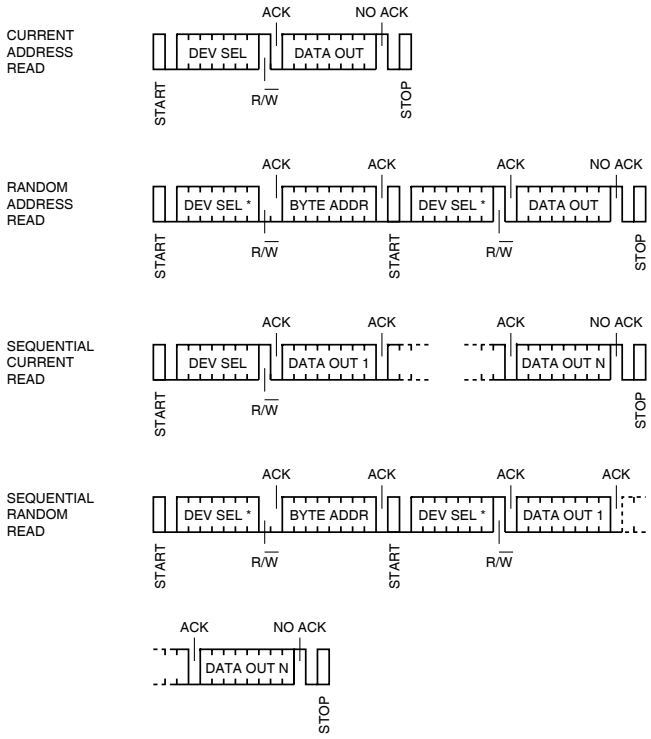
Read operations are independent of the state of the MODE signal. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter (see Figure 11). This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte out-

Figure 11. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

put, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x16 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x16 terminate the data transfer and switches to a standby state.

ORDERING INFORMATION SCHEME

Example: ST24C16 M 1 TR

Operating Voltage	Range	Package	Temperature Range	Option
24 4.5V to 5.5V	C Standard	B PSDIP8 0.25mm Frame	1 0 to 70 °C	TR Tape & Reel Packing
25 2.5V to 5.5V	W Hardware Write Control	M SO8 150mil Width	6 –40 to 85 °C	
			3 (1) –40 to 125 °C	

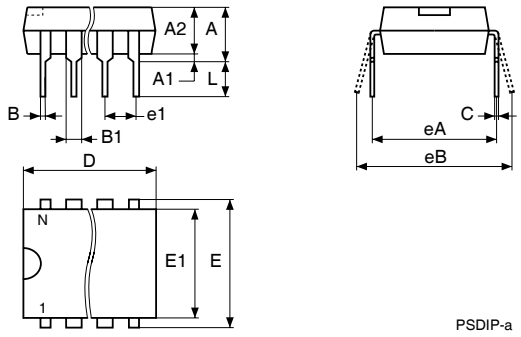
Note: 1. Temperature range on special request only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB		–	10.00		–	0.394
L		3.00	3.80		0.118	0.150
N		8			8	

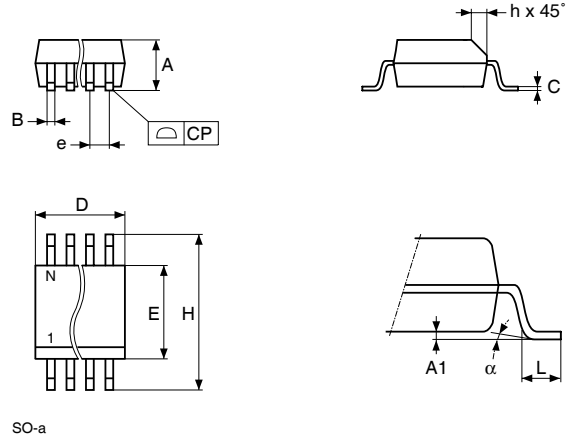


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004



SO-a

Drawing is not to scale.

2 THE I²C-BUS BENEFITS DESIGNERS AND MANUFACTURERS

In consumer electronics, telecommunications and industrial electronics, there are often many similarities between seemingly unrelated designs. For example, nearly every system includes:

- Some intelligent control, usually a single-chip microcontroller
- General-purpose circuits like LCD drivers, remote I/O ports, RAM, EEPROM, or data converters
- Application-oriented circuits such as digital tuning and signal processing circuits for radio and video systems, or DTMF generators for telephones with tone dialling.

To exploit these similarities to the benefit of both systems designers and equipment manufacturers, as well as to maximize hardware efficiency and circuit simplicity, Philips developed a simple bi-directional 2-wire bus for efficient inter-IC control. This bus is called the Inter IC or I²C-bus. At present, Philips' IC range includes more than 150 CMOS and bipolar I²C-bus compatible types for performing functions in all three of the previously mentioned categories. All I²C-bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I²C-bus. This design concept solves the many interfacing problems encountered when designing digital control circuits.

Here are some of the features of the I²C-bus:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- It's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode
- On-chip filtering rejects spikes on the bus data line to preserve data integrity
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

Figure 1 shows two examples of I²C-bus applications.

2.1 Designer benefits

I²C-bus compatible ICs allow a system design to rapidly progress directly from a functional block diagram to a prototype. Moreover, since they 'clip' directly onto the I²C-bus without any additional external interfacing, they allow a prototype system to be modified or upgraded simply by 'clipping' or 'unclipping' ICs to or from the bus.

Here are some of the features of I²C-bus compatible ICs which are particularly attractive to designers:

- Functional blocks on the block diagram correspond with the actual ICs; designs proceed rapidly from block diagram to final schematic.
- No need to design bus interfaces because the I²C-bus interface is already integrated on-chip.
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same IC types can often be used in many different applications
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I²C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced
- Software development time can be reduced by assembling a library of reusable software modules.

In addition to these advantages, the CMOS ICs in the I²C-bus compatible range offer designers special features which are particularly attractive for portable equipment and battery-backed systems.

They all have:

- Extremely low current consumption
- High noise immunity
- Wide supply voltage range
- Wide operating temperature range.

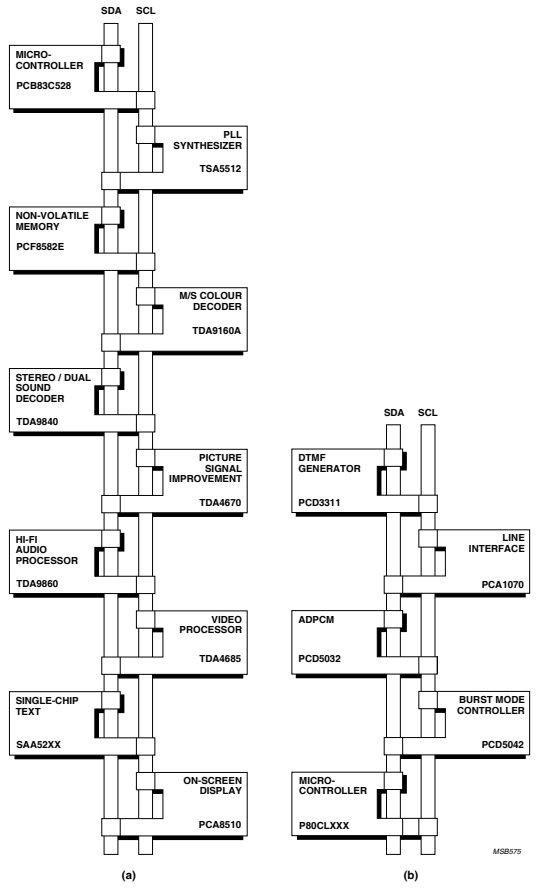


Fig.1 Two examples of I²C-bus applications: (a) a high performance highly-integrated TV set (b) DECT cordless phone base-station.

2.2 Manufacturer benefits

I²C-bus compatible ICs don't only assist designers, they also give a wide range of benefits to equipment manufacturers because:

- The simple 2-wire serial I²C-bus minimizes interconnections so ICs have fewer pins and there are not so many PCB tracks; result - smaller and less expensive PCBs
- The completely integrated I²C-bus protocol eliminates the need for address decoders and other 'glue logic'
- The multi-master capability of the I²C-bus allows rapid testing and alignment of end-user equipment via external connections to an assembly-line
- The availability of I²C-bus compatible ICs in SO (small outline), VSO (very small outline) as well as DIL packages reduces space requirements even more.

These are just some of the benefits. In addition, I²C-bus compatible ICs increase system design flexibility by allowing simple construction of equipment variants and easy upgrading to keep designs up-to-date. In this way, an entire family of equipment can be developed around a basic model. Upgrades for new equipment, or enhanced-feature models (i.e. extended memory, remote control, etc.) can then be produced simply by clipping the appropriate ICs onto the bus. If a larger ROM is needed, it's simply a matter of selecting a micro-controller with a larger ROM from our comprehensive range. As new ICs supersede older ones, it's easy to add new features to equipment or to increase its performance by simply unclipping the outdated IC from the bus and clipping on its successor.

3 INTRODUCTION TO THE I²C-BUS SPECIFICATION

For 8-bit oriented digital control applications, such as those requiring microcontrollers, certain design criteria can be established:

- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders
- The cost of connecting the various devices within the system must be minimized
- A system that performs a control function doesn't require high-speed data transfer
- Overall efficiency depends on the devices chosen and the nature of the interconnecting bus structure.

To produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer IC connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which device will be in control of the bus and when. And, if different devices with different clock speeds are connected to the bus, the bus clock source must be defined. All these criteria are involved in the specification of the I²C-bus.

4 THE I²C-BUS CONCEPT

The I²C-bus supports any IC fabrication process (NMOS, CMOS, bipolar). Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address (whether it's a microcontroller, LCD driver, memory or keyboard interface) and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, whereas a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

Table 1 Definition of I²C-bus terminology

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the winning message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

The I²C-bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually micro-controllers, let's consider the case of a data transfer between two microcontrollers connected to the I²C-bus (see Fig.2).

This highlights the master-slave and receiver-transmitter relationships to be found on the I²C-bus. It should be noted that these relationships are not permanent, but only depend on the direction of data transfer at that time. The transfer of data would proceed as follows:

1) Suppose microcontroller A wants to send information to microcontroller B:

- microcontroller A (master), addresses microcontroller B (slave)
- microcontroller A (master-transmitter), sends data to microcontroller B (slave- receiver)
- microcontroller A terminates the transfer

2) If microcontroller A wants to receive information from microcontroller B:

- microcontroller A (master) addresses microcontroller B (slave)
- microcontroller A (master- receiver) receives data from microcontroller B (slave- transmitter)
- microcontroller A terminates the transfer.

Even in this case, the master (microcontroller A) generates the timing and terminates the transfer.

The possibility of connecting more than one microcontroller to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I²C interfaces to the I²C-bus.

If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see Section 8).

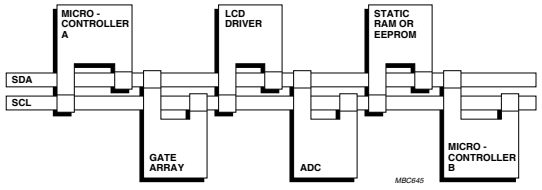


Fig.2 Example of an I²C-bus configuration using two microcontrollers.

Generation of clock signals on the I²C-bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line, or by another master when arbitration occurs.

5 GENERAL CHARACTERISTICS

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a current-source or pull-up resistor (see Fig.3). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I²C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode. The number of interfaces connected to the bus is solely dependent on the bus capacitance limit of 400 pF. For information on High-speed mode master devices, see Section 13.

6 BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, bipolar) which can be connected to the I²C-bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed and depend on the associated level of V_{DD} (see Section 15 for electrical specifications). One clock pulse is generated for each data bit transferred.

6.1 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (see Fig.4).

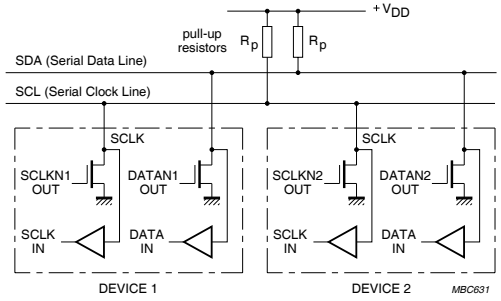


Fig.3 Connection of Standard- and Fast-mode devices to the I²C-bus.

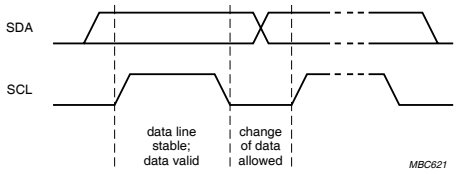


Fig.4 Bit transfer on the I²C-bus.

6.2 START and STOP conditions

Within the procedure of the I²C-bus, unique situations arise which are defined as START (S) and STOP (P) conditions (see Fig.5).

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation is specified in Section 15.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical (see Fig. 10). For the remainder of this document, therefore, the S symbol will be used as a generic term to represent both the START and repeated START conditions, unless Sr is particularly relevant.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period to sense the transition.

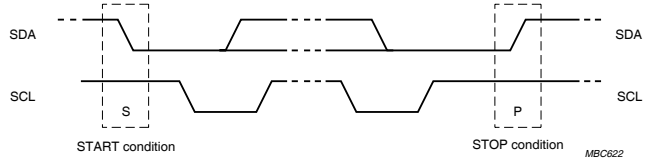


Fig.5 START and STOP conditions.

7 TRANSFERRING DATA

7.1 Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see Fig.6). If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I²C-bus format (for CBUS compatible devices for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see Section 10.1.3).

7.2 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse (see Fig.7). Of course, set-up and hold times (specified in Section 15) must also be taken into account.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received, except when the message starts with a CBUS address (see Section 10.1.3).

When a slave doesn't acknowledge the slave address (for example, it's unable to receive or transmit because it's performing some real-time function), the data line must be left HIGH by the slave. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a slave-receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not-acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates a STOP or a repeated START condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

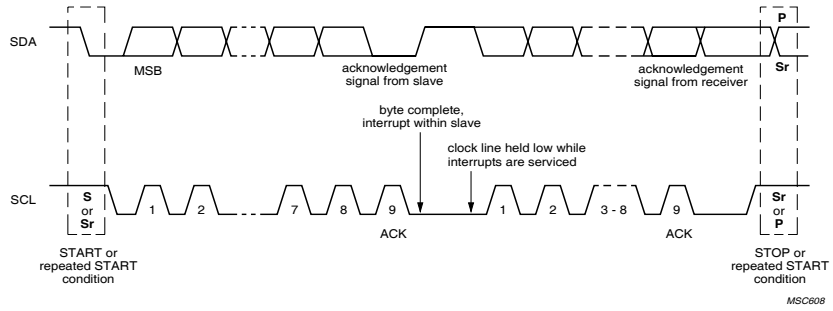


Fig.6 Data transfer on the I²C-bus.

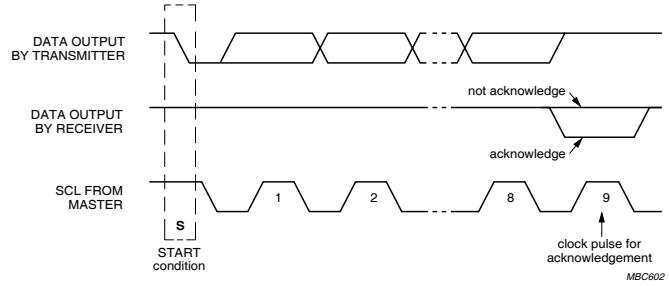


Fig.7 Acknowledge on the I²C-bus.

8 ARBITRATION AND CLOCK GENERATION

8.1 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C-bus. Data is only valid during the HIGH period of the clock. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the devices concerned to start counting off their LOW period and, once a device clock has gone LOW, it will hold the SCL line in that state until the clock HIGH state is reached (see Fig.8). However, the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. The SCL line will therefore be held LOW by the device with the longest LOW period. Devices with shorter LOW periods enter a HIGH wait-state during this time.

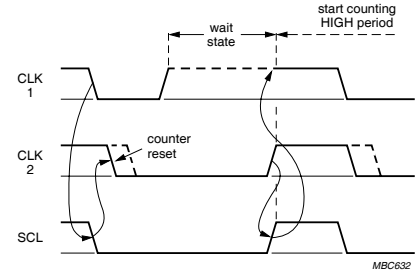


Fig.8 Clock synchronization during the arbitration procedure.

When all devices concerned have counted off their LOW period, the clock line will be released and go HIGH. There will then be no difference between the device clocks and the state of the SCL line, and all the devices will start counting their HIGH periods. The first device to complete its HIGH period will again pull the SCL line LOW.

In this way, a synchronized SCL clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

8.2 Arbitration

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition within the minimum hold time ($t_{HD;STA}$) of the START condition which results in a defined START condition to the bus.

Arbitration takes place on the SDA line, while the SCL line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output stage because the level on the bus doesn't correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits (addressing information is given in Sections 10 and 14). If the masters are each trying to address the same device, arbitration continues with comparison of the data-bits if they are master-transmitter, or acknowledge-bits if they are master-receiver. Because address and data information on the I²C-bus is determined by the winning master, no information is lost during the arbitration process.

A master that loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

As an Hs-mode master has a unique 8-bit master code, it will always finish the arbitration during the first byte (see Section 13).

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it's possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave mode.

Figure 9 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a HIGH output level is then connected to the bus. This will not affect the data transfer initiated by the winning master.

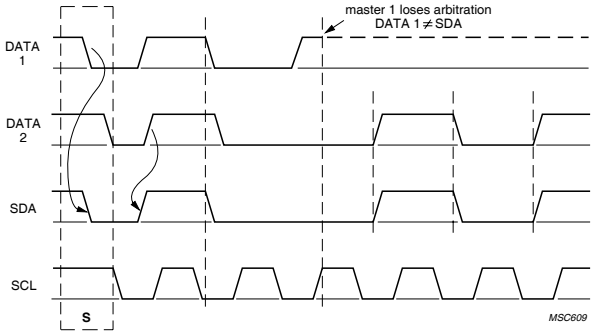


Fig.9 Arbitration procedure of two masters.

Since control of the I²C-bus is decided solely on the address or master code and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I²C-bus. If it's possible for such a situation to occur, the masters involved must send this repeated START condition or STOP condition at the same position in the format frame. In other words, arbitration isn't allowed between:

- A repeated START condition and a data bit
- A STOP condition and a data bit
- A repeated START condition and a STOP condition.

Slaves are not involved in the arbitration procedure.

8.3 Use of the clock synchronizing mechanism as a handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receivers to cope with fast data transfers, on either a byte level or a bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the SCL line LOW after reception and acknowledgment of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure (see Fig.6).

On the bit level, a device such as a microcontroller with or without limited hardware for the I²C-bus, can slow down the bus clock by extending each clock LOW period. The speed of any master is thereby adapted to the internal operating rate of this device.

In Hs-mode, this handshake feature can only be used on byte level (see Section 13).

9 FORMATS WITH 7-BIT ADDRESSES

Data transfers follow the format shown in Fig.10. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/$\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

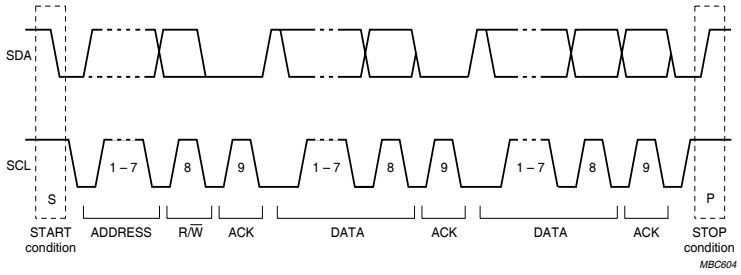


Fig.10 A complete data transfer.

Possible data transfer formats are:

- Master-transmitter transmits to slave-receiver. The transfer direction is not changed (see Fig.11).
- Master reads slave immediately after first byte (see Fig.12). At the moment of the first acknowledge, the master- transmitter becomes a master- receiver and the slave-receiver becomes a slave-transmitter. This first acknowledge is still generated by the slave. The STOP condition is generated by the master, which has previously sent a not-acknowledge ($\overline{A}$).
- Combined format (see Fig.13). During a change of direction within a transfer, the START condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed. If a master receiver sends a repeated START condition, it has previously sent a not-acknowledge ($\overline{A}$).

NOTES:

1. Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2. All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3. Each byte is followed by an acknowledgment bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4. I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address, even if these START conditions are not positioned according to the proper format.
5. A START condition immediately followed by a STOP condition (void message) is an illegal format.

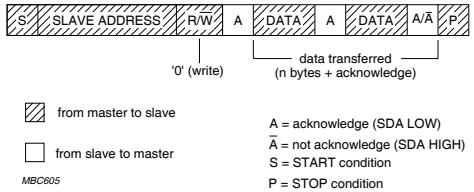


Fig.11 A master-transmitter addressing a slave receiver with a 7-bit address. The transfer direction is not changed.

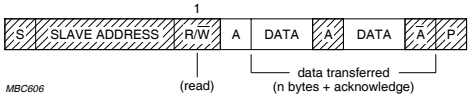


Fig.12 A master reads a slave immediately after the first byte.

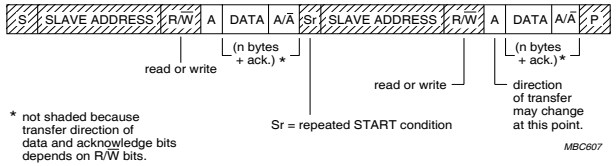


Fig.13 Combined format.

10 7-BIT ADDRESSING

The addressing procedure for the I²C-bus is such that the first byte after the START condition usually determines which slave will be selected by the master. The exception is the 'general call' address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge. However, devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken. This procedure is explained in more detail in Section 10.1.1. For information on 10-bit addressing, see Section 14

10.1 Definition of bits in the first byte

The first seven bits of the first byte make up the slave address (see Fig.14). The eighth bit is the LSB (least significant bit). It determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/$\overline{W}$ bit.

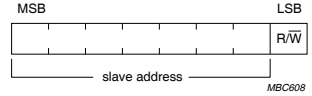


Fig.14 The first byte after the START procedure.

A slave address can be made-up of a fixed and a programmable part. Since it's likely that there will be several identical devices in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C-bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of 8 identical devices can be connected to the same bus.

The I²C-bus committee coordinates allocation of I²C addresses. Further information can be obtained from the Philips representatives listed on the back cover. Two groups of eight addresses (0000XXX and 1111XXX) are reserved for the purposes shown in Table 2. The bit combination 11110XX of the slave address is reserved for 10-bit addressing (see Section 14).

Table 2 Definition of bits in the first byte

SLAVE ADDRESS	R/$\overline{W}$ BIT	DESCRIPTION
0000 000	0	General call address
0000 000	1	START byte(1)
0000 001	X	CBUS address(2)
0000 010	X	Reserved for different bus format(3)
0000 011	X	Reserved for future purposes
0000 1XX	X	Hs-mode master code
1111 1XX	X	Reserved for future purposes
1111 0XX	X	10-bit slave addressing

Notes

1. No device is allowed to acknowledge at the reception of the START byte.
2. The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I²C-bus compatible devices in the same system. I²C-bus compatible devices are not allowed to respond on reception of this address.
3. The address reserved for a different bus format is included to enable I²C and other protocols to be mixed. Only I²C-bus compatible devices that can work with such formats and protocols are allowed to respond to this address.

10.1.1 General call address

The general call address is for addressing every device connected to the I²C-bus. However, if a device doesn't need any of the data supplied within the general call structure, it can ignore this address by not issuing an acknowledgment. If a device does require data from a general call address, it will acknowledge this address and behave as a slave- receiver. The second and following bytes will be acknowledged by every slave- receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not-acknowledging. The meaning of the general call address is always specified in the second byte (see Fig.15).

There are two cases to consider:

- When the least significant bit B is a 'zero'.
- When the least significant bit B is a 'one'.

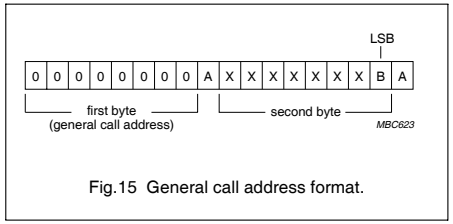


Fig.15 General call address format.

When bit B is a 'zero'; the second byte has the following definition:

- 00000110 (H'06'). Reset and write programmable part of slave address by hardware. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address. Pre-cautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.
- 00000100 (H'04'). Write programmable part of slave address by hardware. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The device will not reset.
- 00000000 (H'00'). This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore them.

When bit B is a 'one'; the 2-byte sequence is a 'hardware general call'. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master doesn't know in advance to which device the message has to be transferred, it can only generate this hardware general call and its own address - identifying itself to the system (see Fig.16).

The seven bits remaining in the second byte contain the address of the hardware master. This address is recognized by an intelligent device (e.g. a microcontroller) connected to the bus which will then direct the information from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

14.3 General call address and start byte with 10-bit addressing

The 10-bit addressing procedure for the I²C-bus is such that the first two bytes after the START condition (S) usually determine which slave will be selected by the master. The exception is the "general call" address 00000000 (H'00'). Slave devices with 10-bit addressing will react to a "general call" in the same way as slave devices with 7-bit addressing (see Section 10.1.1).

Hardware masters can transmit their 10-bit address after a 'general call'. In this case, the 'general call' address byte is followed by two successive bytes containing the 10-bit address of the master-transmitter. The format is as shown in Fig.10 where the first DATA byte contains the eight least-significant bits of the master address.

The START byte 00000001 (H'01') can precede the 10-bit addressing in the same way as for 7-bit addressing (see Section 10.1.2).

15 ELECTRICAL SPECIFICATIONS AND TIMING FOR I/O STAGES AND BUS LINES

15.1 Standard- and Fast-mode devices

The I/O levels, I/O current, spike suppression, output slope control and pin capacitance for F/S-mode I²C-bus devices are given in Table 4. The I²C-bus timing characteristics, bus-line capacitance and noise margin are given in Table 5. Figure 31 shows the timing definitions for the I²C-bus.

The minimum HIGH and LOW periods of the SCL clock specified in Table 5 determine the maximum bit transfer rates of 100 kbit/s for Standard-mode devices and 400 kbit/s for Fast-mode devices. Standard-mode and Fast-mode I²C-bus devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure described in Section 8 which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Table 4 Characteristics of the SDA and SCL I/O stages for F/S-mode I²C-bus devices

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 –0.5 –0.5	 1.5 $0.3V_{DD}$	 n/a –0.5	 n/a $0.3V_{DD}$ (1)	 V V
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 (2) (2)	 n/a $0.7V_{DD}$(1)	 n/a (2)	 V V
Hysteresis of Schmitt trigger inputs: V_{DD} > 2 V V_{DD} < 2 V	V_{hys}	 n/a n/a	 n/a n/a	 $0.05V_{DD}$ $0.1V_{DD}$	 – –	 V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: V_{DD} > 2 V V_{DD} < 2 V	 V_{OL1} V_{OL3}	 0 n/a	 0.4 n/a	 0 0	 0.4 $0.2V_{DD}$	 V V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	t_{of}	–	250(4)	$20 + 0.1C_b$(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	–10	10	–10(5)	10(5)	µA
Capacitance for each I/O pin	C_i	–	10	–	10	pF

Notes

1. Devices that use non-standard supply voltages which do not conform to the intended I²C-bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5$ V.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table 5 (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.36 without exceeding the maximum specified t_f.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

n/a = not applicable

Table 5 Characteristics of the SDA and SCL bus lines for F/S-mode I²C-bus devices(1)

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

Notes

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 4).
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 6 are allowed.

n/a = not applicable

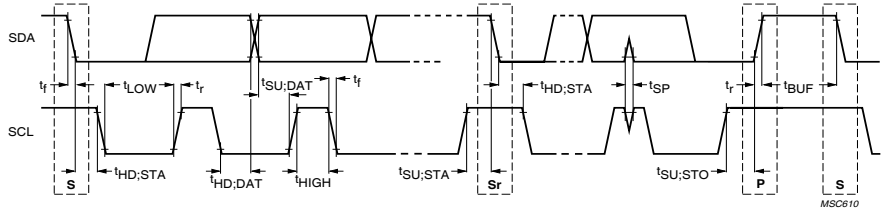


Fig.31 Definition of timing for F/S-mode devices on the I²C-bus.

16 ELECTRICAL CONNECTIONS OF I²C-BUS DEVICES TO THE BUS LINES

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Section 15.

I²C-bus devices with fixed input levels of 1.5 V and 3 V can each have their own appropriate supply voltage. Pull-up resistors must be connected to a 5 V ± 10% supply (Fig.33). I²C-bus devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig.34).

When devices with fixed input levels are mixed with devices with input levels related to V_{DD}, the latter devices must be connected to one common supply line of 5 V ± 10% and must have pull-up resistors connected to their SDA and SCL pins as shown in Fig.35.

New Fast- and Hs-mode devices must have supply voltage related input levels as specified in Tables 4 and 6.

Input levels are defined in such a way that:

- The noise margin on the LOW level is $0.1V_{DD}$
- The noise margin on the HIGH level is $0.2V_{DD}$
- As shown in Fig.36, series resistors (R_S) of e.g. 300 Ω can be used for protection against high-voltage spikes on the SDA and SCL lines (resulting from the flash-over of a TV picture tube, for example).

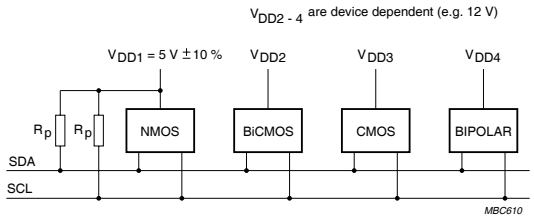


Fig.33 Fixed input level devices connected to the I²C-bus.

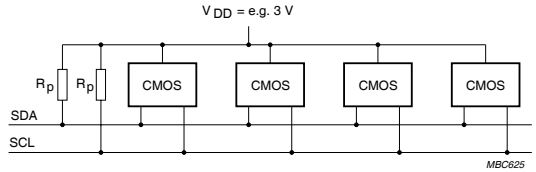


Fig.34 Devices with wide supply voltage range connected to the I²C-bus.

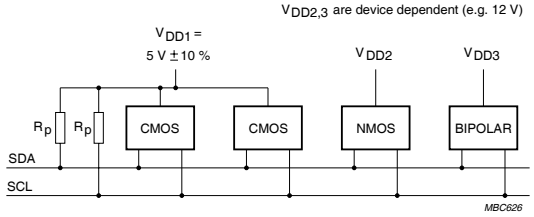


Fig.35 Devices with input levels related to V_{DD} (supply V_{DD1}) mixed with fixed input level devices (supply $V_{DD2,3}$) on the I²C-bus.

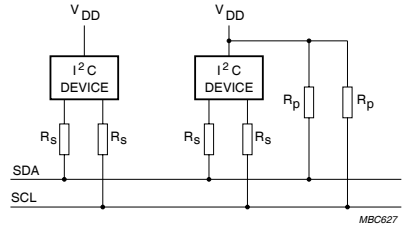


Fig.36 Series resistors (R_s) for protection against high-voltage spikes.

16.1 Maximum and minimum values of resistors R_p and R_s for Standard-mode I²C-bus devices

For Standard-mode I²C-bus systems, the values of resistors R_p and R_s in Fig.33 depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current).

The supply voltage limits the minimum value of resistor R_p due to the specified minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages. V_{DD} as a function of $R_{p\,min}$ is shown in Fig.37. The required noise margin of $0.1V_{DD}$ for the LOW level, limits the maximum value of R_s. $R_{s\,max}$ as a function of R_p is shown in Fig.38.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time. Fig.39 shows $R_{p\,max}$ as a function of bus capacitance.

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 μA. Due to the required noise margin of 0.2 V_{DD} for the HIGH level, this input current limits the maximum value of R_p. This limit depends on V_{DD}. The total HIGH level input current is shown as a function of $R_{p\,max}$ in Fig.40.

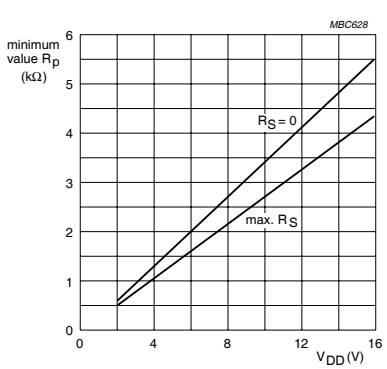


Fig.37 Minimum value of R_p as a function of supply voltage with the value os R_s as a parameter.

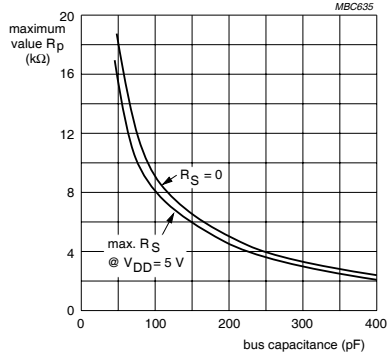


Fig.39 Maximum value of R_p as a function of bus capacitance for a Standard-mode I²C-bus.

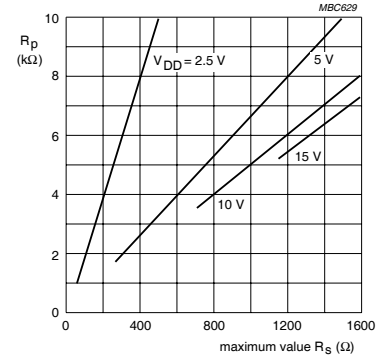


Fig.38 Maximum value of R_s as a function of the value of R_p with supply voltage as a parameter.

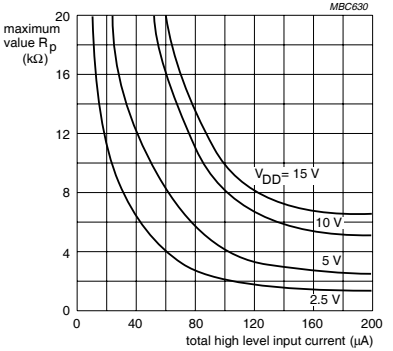


Fig.40 Total HIGH level input current as a function of the maximum value of R_p with supply voltage as a parameter.

I²C-BUS ALLOCATION TABLE (IN GROUP ORDER)

The group number represents the hexadecimal equivalent of the four most significant bits of the slave address (A6-A3).

GROUP[1]			TYPE NUMBER	DESCRIPTION
Group 0 (0000)				
0	0	0	-	General call address
X	X	X	-	Reserved addresses
Group 1 (0001)				
1	A1	A0	SAA2530	ADR/DMX digital receiver
1	A1	A0	TDA8045	QAM-64 demodulator
Group 2 (0010)				
0	0	A0	SAA4700/T	VPS dataline processor
0	0	A0	SAA5233	Dual standard PDC decoder
0	0	1	SAA5243	Computer controlled teletext circuit
0	0	1	SAA5244	Integrated VIP and teletext
0	0	1	SAA5245	525-line teletext decoder/controller
0	0	1	SAA5246A	Integrated VIP and teletext
0	0	1	SAA5249	VIP and teletext controller
0	A1	A0	CCR921	RDS/RBDS decoder
0	A1	A0	SAF1135	Dataline 16 decoder for VPS (call array)
1	0	0	SAA5252	Line 21 decoder
1	1	A0	SAB9075H	PIP controller for NTSC
Group 3 (0011)				
0	0	A0	SAA7370	CD-decoder plus digital servo processor
0	A1	A0	PCD5096	Universal codec
0	1	A0	SAA2510	Video-CD MPEG-audio/video decoder
0	1	1	PDIUSB11	Universal serial bus
1	0	1	SAA2502	MPEG audio source decoder
1	1	A0	SAA1770	D2MAC decoder for satellite and cable TV
Group 4 (0100)				
0	0	0	SAA6750	MPEG2 encoder for Desk Top Video (=SAA7137)
0	0	0	TDA9177	YUV transient improvement processor
0	0	0	TDA9178	YUV transient improvement processor
0	0	A0	PCA1070	Programmable speech transmission IC
0	A1	A0	SAA1300	Tuner switch circuit
A2	A1	A0	TDA8444	Octuple 6-bit DAC
A2	A1	A0	PCF8574	8-bit remote I/O port (I²C-bus to parallel converter)
1	0	A0	PCD3311C	DTMF/modem/musical tone generator
1	0	A0	PCD3312C	DTMF/modem/musical tone generator
1	1	1	PCD5002	Pager decoder

GROUP[1]			TYPE NUMBER	DESCRIPTION
Group 5 (0110)				
0	0	0	SAA5301	MOJI processor for Japan/China
0	1	1	PCE84C467/8	8-bit CMOS auto-sync monitor controller
0	1	1	PCE84C882	8-bit microcontroller for monitor applications
0	1	1	PCE84C886	8-bit microcontroller for monitor applications
Group 7 (0111)				
0	0	A0	SAA7140B	High performance video scaler
0	0	A0	PCF8576C	16-segment LCD driver 1:1 - 1:4 Mux rates
0	A1	A0	SAA1064	4-digit LED driver
A2	A1	A0	PCF8574A	8-bit remote I/O port (I²C-bus to parallel converter)
0	1	0	PCF8577C	32/64-segment LCD display driver
0	1	A0	SAA2118	LCD controller/driver
1	0	A0	PCF8578/9	Row/column LCD dot matrix driver/display
1	0	A0	PCF8568	LCD row driver for dot matrix displays
1	0	A0	PCF8569	LCD column driver for dot matrix displays
1	1	A0	PCF8566	96-segment LCD driver 1:1 - 1:4 Mux rates
Group 8 (1000)				
0	0	0	TEA6300	Sound fader control and preamplifier/source selector
0	0	0	TEA6320/1/2/3	Sound fader control circuit
0	0	0	TEA6330	Tone/volume controller
0	0	A0	NE5751	Audio processor for RF communication
0	0	A0	TDA8421	Audio processor
0	0	A0	TDA9860	HI-fi audio processor
0	0	1	TDA8424/5/6	Audio processor
0	1	0	TDA8415	TV/VCR stereo/dual sound processor
0	1	0	TDA8417	TV/VCR stereo/dual sound processor
0	1	0	TDA9840	TV stereo/dual sound processor
0	1	A0	TDA8480T	RGB gamma-correction processor
1	0	0	TDA4670/1/2	Picture signal improvement (PSI) circuit
1	0	0	TDA4880/5/7/8	Video processor
1	0	0	TDA4780	Video control with gamma control
1	0	0	TDA4885	150 MHz video controller
1	0	0	TDA8442	Interface for colour decoder
1	0	1	TDA8386	Multistandard one-chip video processor
1	0	1	TDA8373	NTSC one-chip video processor
1	0	1	TDA8374	Multistandard one-chip video processor
1	0	1	TDA8375/A	Multistandard one-chip video processor
1	0	1	TDA8376/A	Multistandard one-chip video processor
1	0	1	TDA9161A	Bus-controlled decoder/sync. processor
1	A1	1	SAA7151B	8-bit digital multistandard TV decoder

GROUP[1]			TYPE NUMBER	DESCRIPTION
1	A1	1	SAA7191B	Digital multistandard TV decoder
1	A1	1	SAA9056	Digital SCAM colour decoder
1	A1	1	TDA9141/3/4	Alignment-free multistandard decoder
1	A1	1	TDA9160	Multistandard decoder/sync. processor
1	A1	1	TDA9162	Multistandard decoder/sync. processor
1	1	0	TDA4853/4	Autosync deflection processor
1	1	0	TDA9150B	Deflection processor
1	1	0	TDA9151B	Programmable deflection processor
1	1	A0	TEA6360	5-band equalizer
1	1	A0	TDA8433	TV deflection processor
Group 9 (1001)				
A2	A1	A0	PCF8591	4-channel, 8-bit Mux ADC and one DAC
A2	A1	A0	TDA8440	Video/audio switch
A2	A1	A0	TDA8540	4 × 4 video switch matrix
1	A1	A0	TDA8752	Triple fast ADC for LCD
1	1	A0	SAA7110A	Digital multistandard decoder
Group A (1010)				
0	0	0	PCB2421	1K dual mode serial EEPROM
0	0	A0	PCF8583	256 × 8-bit RAM/clock/calendar
0	0	1	PCF8593	Low-power clock calender
A2	A1	A0	PCF8570	256 × 8-bit static RAM
A2	A1	A0	PCF8522/4	512 × 8-bit CMOS EEPROM
A2	A1	A0	PCA8581/C	128 × 8-bit EEPROM
A2	A1	A0	PCF8582/A	256 × 8-bit EEPROM
A2	A1	P0	PCX8594	512 × 8-bit CMOS EEPROM
A2	P1	P0	PCX8598	1024 × 8-bit CMOS EEPROM
Group B (1011)				
0	0	A0	SAA7199B	Digital multistandard encoder
0	1	0	TDA8418	TV/VCR stereo/dual sound processor
0	1	A0	TDA9850	BTSC stereo/SAP decoder
0	1	A0	TDA9855	BTSC stereo/SAP decoder
0	1	1	TDA9852	BTSC stereo/SAP decoder
1	0	0	TDA9810	Audio FM processor for VHS
1	0	0	TDA9814H	Audio processor for VHS
1	A1	0	SAA7186	Digital video scaler
1	0	1	PCA8516	Stand-alone OSD IC
1	1	1	SAA7185	Video enhancement D/A processor
1	1	1	SAA9065	Video enhancement and D/A processor
Group C (1100)				
0	0	1	TEA6100	FM/IF for computer-controlled radio

GROUP[1]			TYPE NUMBER	DESCRIPTION
0	1	0	TEA6821/2	Car radio AM
0	1	0	TEA6824T	Car radio IF IC
0	A1	A0	TSA5511/2/4	1.3 GHz PLL frequency synthesizer for TV
0	A1	A0	TSA5522/3M	1.4 GHz PLL frequency synthesizer for TV
0	1	A0	TDA8735	150 MHz PLL frequency synthesizer
0	1	A0	TSA6057	Radio tuning PLL frequency synthesizer
0	1	A0	TSA6060	Radio tuning PLL frequency synthesizer
0	1	A0	UMA1014	Frequency synthesizer for mobile telephones
1	0	0	TDA8722	Negative video modulator with FM sound
Group D (1101)				
0	0	A0	TDA8043	QPSK demodulator and decoder
0	0	A0	TDA9170	YUV processor with picture improvement
0	A1	A0	PCF8573	Clock/calendar
A2	A1	A0	TDA8443A	YUV/RGB matrix switch
0	1	A0	TDA8745	Satellite sound decoder
1	0	0	TDA1551Q	2 × 22 W BTL audio power amplifier
1	A1	A0	TDA4845	Vector processor for TV-pictures tubes
1	A1	A0	UMA1000T	Data processor for mobile telephones
1	1	A0	PCD4440	Voice scrambler/descrambler for mobile telephones
Group E (1110)				
0	0	0	TDA9177	2nd address for LTI (1st is '40')
0	0	0	TDA9178	2nd address for LTI (1st is '40')
0	0	A0	SAA7192	Digital colour space-converter
Group F (1111)				
X	X	X	-	Reserved addresses
Group 0 to F (0000 to 1111)				
X	X	X	PCF8584	I²C-bus controller

Note

1. X = Don't care, A = Programmable address bit, P = Page selection bit

1 FEATURES

- Parallel-bus to I²C-bus protocol converter and interface
- Compatible with most parallel-bus microcontrollers/microprocessors including 8049, 8051, 6800, 68000 and Z80
- Both master and slave functions
- Automatic detection and adaption to bus interface type
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode (4-wire)
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range: −40 to +85 °C.

2 GENERAL DESCRIPTION

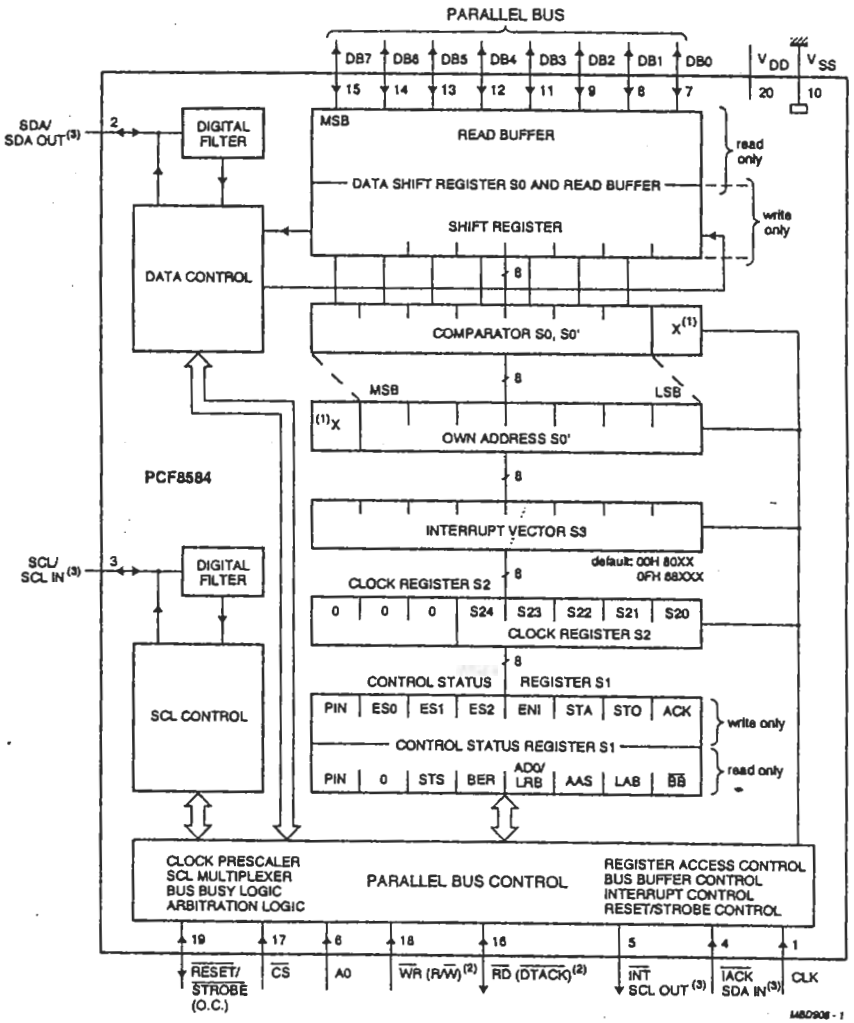
The PCF8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/microprocessors and the serial I²C-bus. The PCF8584 provides both master and slave functions.

Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequences, protocol, arbitration and timing. The PCF8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8584P	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCF8584T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4 BLOCK DIAGRAM

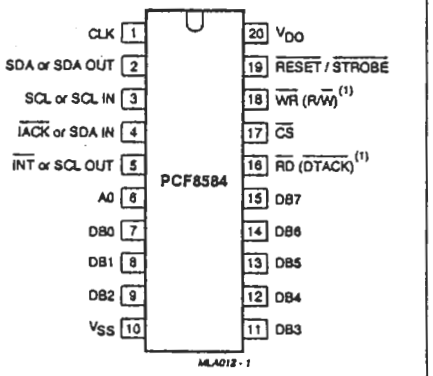


(1) X = don't care.
(2) Pin mnemonics between parenthesis indicate the 68000 mode pin designations.
(3) These pin mnemonics represent the long-distance mode pin designations.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
CLK	1	I	clock input from microcontroller clock generator (internal pull-up)
SDA or SDA OUT	2	I/O	I²C-bus serial data input/output (open-drain). Serial data output in long-distance mode.
SCL or SCL IN	3	I/O	I²C-serial clock input/output (open-drain). Serial clock input in long-distance mode.
$\overline{IACK}$ or SDA IN	4	I	Interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in register S3 will be available at the bus Port if the ENI flag is set. Serial data input in long-distance mode.
$\overline{INT}$ or SCL OUT	5	O	Interrupt output (open-drain); this signal is enabled by the ENI flag in register S1. It is asserted when the PIN flag is reset. (PIN is reset after 1 byte is transmitted or received over the I²C-bus). Serial clock output in long-distance mode.
A0	6	I	Register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects register S1, logic 0 selects one of the other registers depending on bits loaded in ES0, ES1 and ES2 of register S1.
DB0	7	I/O	bidirectional 8-bit bus Port 0
DB1	8	I/O	bidirectional 8-bit bus Port 1
DB2	9	I/O	bidirectional 8-bit bus Port 2
V_{SS}	10	–	ground
DB3	11	I/O	bidirectional 8-bit bus Port 3
DB4	12	I/O	bidirectional 8-bit bus Port 4
DB5	13	I/O	bidirectional 8-bit bus Port 5
DB6	14	I/O	bidirectional 8-bit bus Port 6
DB7	15	I/O	bidirectional 8-bit bus Port 7
$\overline{RD}$ ($\overline{DTACK}$)	16	I/(O)	$\overline{RD}$ is the read control input for MAB8049, MAB8051 or Z80-types. $\overline{DTACK}$ is the data transfer control output for 68000-types (open-drain).
$\overline{CS}$	17	I	chip select input (internal pull-up)
$\overline{WR}$ (R/$\overline{W}$)	18	I	$\overline{WR}$ is the write control input for MAB8048, MAB8051, or Z80-types (internal pull-up). R/$\overline{W}$ control input for 68000-types.
$\overline{RESET}$/ $\overline{STROBE}$	19	I/O	Reset input (open-drain); this input forces the I²C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.
V_{DD}	20	–	supply voltage



(1) Pin mnemonics between parenthesis indicate the 68000 mode pin designations.

Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 General

The PCF8584 acts as an interface device between standard high-speed parallel buses and the serial I²C-bus. On the I²C-bus, it can act either as master or slave. Bidirectional data transfer between the I²C-bus and the parallel-bus microcontroller is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. 8048, 8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed (see Section 6.2).

Table 1 Control signals utilized by the PCF8584 for microcontroller/microprocessor interfacing

TYPE	R/$\overline{W}$	$\overline{WR}$	$\overline{R}$	$\overline{DTACK}$	$\overline{IACK}$
8048/ 8051	no	yes	yes	no	no
68000	yes	no	no	yes	yes
Z80	no	yes	yes	no	yes

The structure of the PCF8584 is similar to that of the I²C-bus interface section of the Philips' MABXXXX/PCF84(C)XX-series of microcontrollers, but with a modified control structure. The PCF8584 has five internal register locations. Three of these (own address register S0', clock register S2 and interrupt vector S3) are used for initialization of the PCF8584. Normally they are only written once directly after resetting of the PCF8584.

The remaining two registers function as double registers (data buffer/shift register S0, and control/status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. Register S0 is a combination of a shift register and data buffer.

Register S0 performs all serial-to-parallel interfacing with the I²C-bus.

Register S1 contains I²C-bus status information required for bus access and/or monitoring.

6.2 Interface Mode Control (IMC)

Selection of either an 80XX mode or 68000 mode interface is achieved by detection of the first $\overline{WR}$-$\overline{CS}$ signal sequence. The concept takes advantage of the fact that the write control input is common for both types of interfaces. An 80XX-type interface is default. If a HIGH-to-LOW transition of $\overline{WR}$ (R/$\overline{W}$) is detected while $\overline{CS}$ is HIGH, the 68000-type interface mode is selected and the $\overline{DTACK}$ output is enabled. Care must be taken that $\overline{WR}$ and $\overline{CS}$ are stable after reset.

Hi-fi stereo audio processor; I²C-bus TDA8425

GENERAL DESCRIPTION

The TDA8425 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I²C-bus for application in hi-fi audio and television sound.

Feature:

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity					
full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	–64	–	6	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146); SOT146-1; 1996 November 26.

Hi-fi stereo audio processor; I²C-bus TDA8425

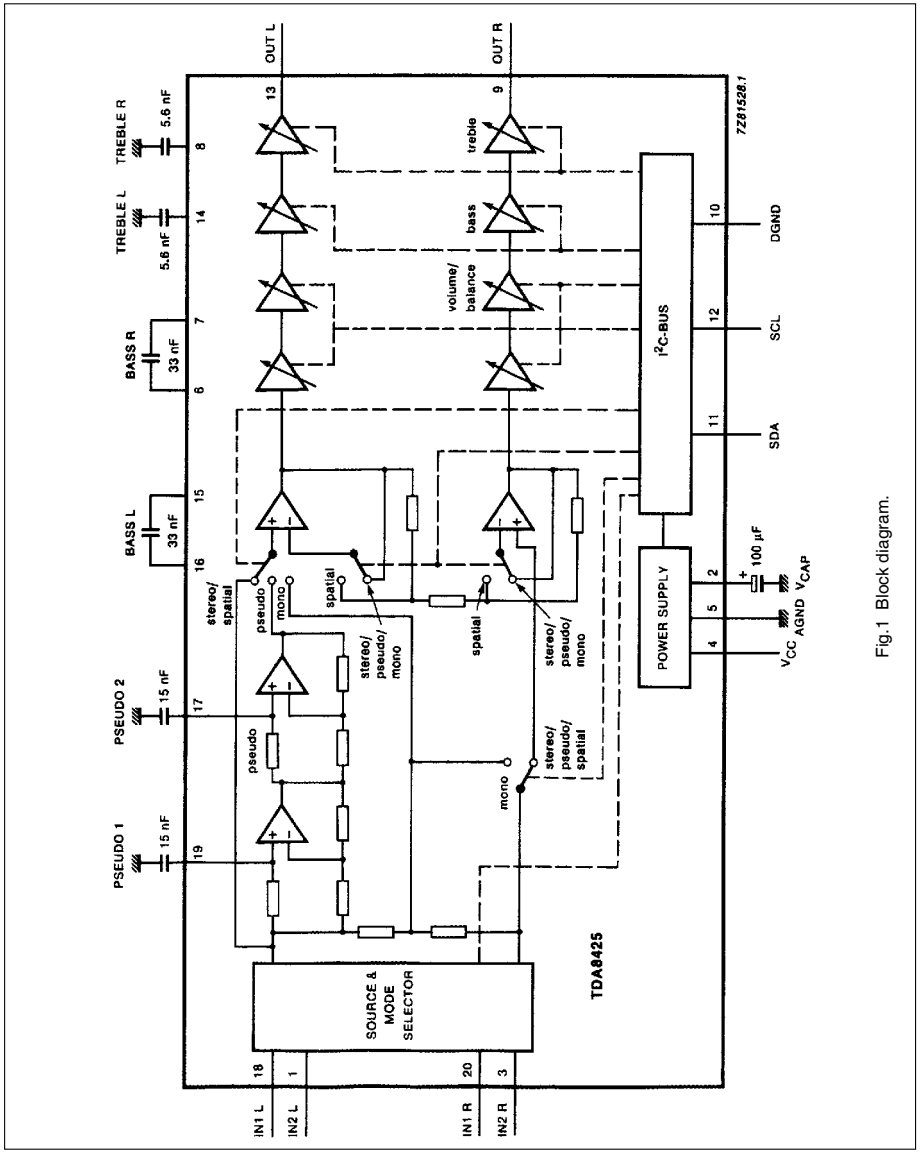


Fig.1 Block diagram.

PINNING

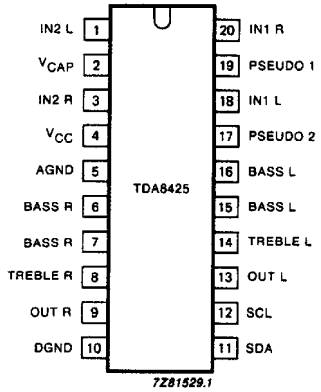


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN 1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and –64 dB in steps of 2 dB. An additional step allows an attenuation of ≥ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode(1)

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

(1) During forced mono mode the pseudo stereo mode cannot be used.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from +12 dB to –12 dB in steps of 3 dB.

Bias and power supply

The TDA8425 includes a bias and power supply stage, which generates a voltage of $0.5 \times V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I²C-bus receiver and data handling

Bus specification

The TDA8425 is controlled via the 2-wire I²C-bus by a microcomputer.
The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8425 starts with the module address MAD.

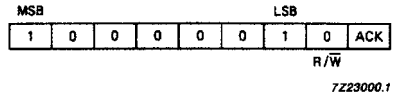


Fig.3 TDA8425 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8425. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig.5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8425. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

		MSB							LSB
function		7	6	5	4	3	2	1	0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono[1]	0	0

Table 5 Mute

mute	MU
active; automatic	
after POR[2]	1
not active	0

Notes

1. Pseudo stereo function is not possible in this mode.
2. Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V × 5	V × 4	V × 3	V × 2	V × 1	V × 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
–62	0	1	1	1	0	1
–64	0	1	1	1	0	0
≤ –80	0	1	1	0	1	1
≤ –80	0	0	0	0	0	0

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
15	1	0	1	1
12	1	0	1	0
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
0	0	1	1	0
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
−12	0	0	1	0
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
12	1	0	1	0
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
0	0	1	1	0
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
−12	0	0	1	0
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
. .	. .	. .	. .	. .
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

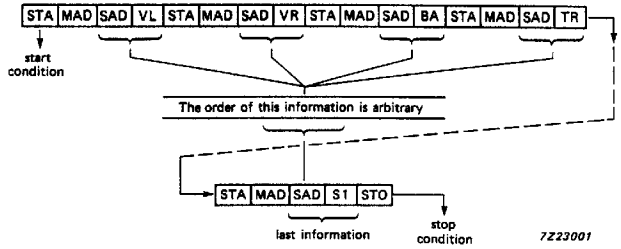


Fig.4 Data transmission after a power-on reset.

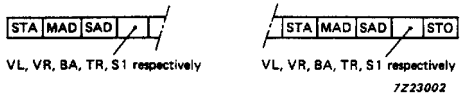


Fig.5 Data transmission after a power-on reset with auto increment.

Fig.6 Data transmission except after power-on reset.