AGREGATION INTERNE DE GENIE ELECTRIQUE

Option A

ELECTRONIQUE ET INFORMATIQUE INDUSTRIELLE

Etude d'un système industriel (durée 8 heures)

PILOTAGE D'UN FOUR ELECTRIQUE A ARC

DOCUMENTS CONSTRUCTEUR

Ce document présente les documentations partielles des composants nécessaires.

PMI

OP-20

MICROPOWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

Precision Monolithics Inc.

FEATURES

- Low Supply Current ..... 55μA Max
- Single-Supply Operation ..... +5V to +30V
- Dual-Supply Operation ..... ±2.5V to ±15V
- Low Input Offset Voltage ..... 250μV Max
- Low Input Offset Voltage Drift ..... 1.5μV/°C Max
- High Common-Mode Input Range ... V− to V+ (−1.5V)
- High CMRR and PSRR ..... 100dB Min
- High Open-Loop Gain ..... 120dB Min
- No External Components Required
- 741 Pinout and Nulling

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
250	OP20BJ*	OP20BZ*		MIL
250	OP20FJ	OP20FZ		IND
250			OP20FP	COM
500	OP20CJ*	OP20CZ*		MIL
500	OP20GJ	OP20GZ		IND
500			OP20GP	COM
1000	OP20HJ	OP20HZ	OP20HP	COM

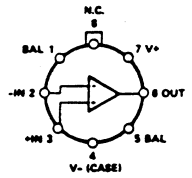
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

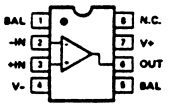
The OP-20 is a monolithic micropower operational amplifier that can be operated from a single power supply of +5V to +30V, or from dual supplies of ±2.5V to ±15V. The input voltage range extends to the negative rail, therefore input signals down to zero volts can be accomodated when operating from a single supply.

Precision performance in high-gain applications is readily obtained when using the OP-20. The B/F grade features a maximum input offset voltage of 250μV, minimum CMRR of 95dB, and open-loop gain of over 500,000. Quiescent supply current is a maximum of only 55μA at ±2.5V or 80μA at ±15V. The low input offset, high gain, and low power consumption brings precision performance to portable instruments, satellites, missile control systems, and many other battery-powered applications.

PIN CONNECTIONS

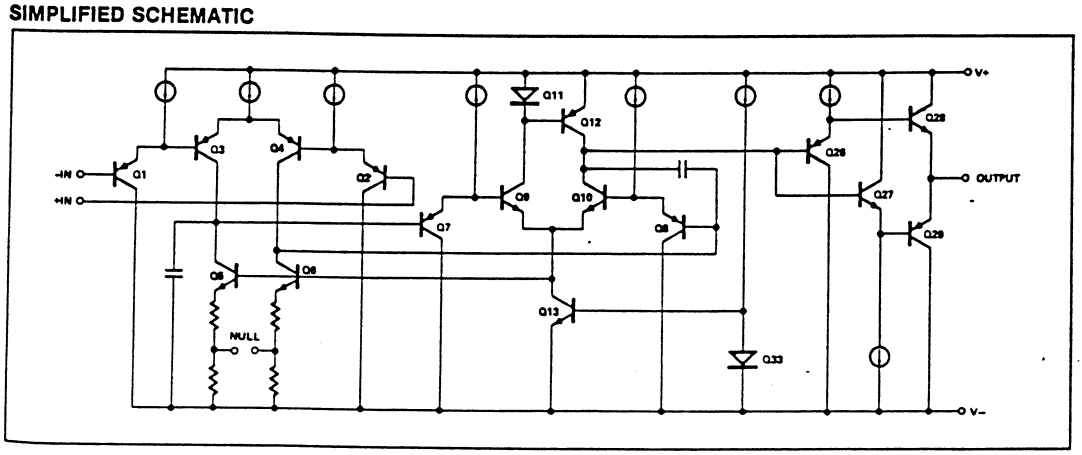


TO-99
(J-Suffix)



EPOXY MINI-DIP
(P-Suffix)
And
8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Power Dissipation 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J and Z Packages ..... −65°C to +150°C
P Package ..... −65°C to +125°C

Operating Temperature Range
OP-20B, OP-20C (J or Z package) ... −55°C to +125°C
OP-20F, OP-20G (J or Z package) .... −25°C to +85°C
OP-20FP, OP-20GP, OP-20HP
OP-20HJ, OP-20HZ ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTE:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20B/F MIN	OP-20B/F TYP	OP-20B/F MAX	OP-20C/G MIN	OP-20C/G TYP	OP-20C/G MAX	OP-20H MIN	OP-20H TYP	OP-20H MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	55	250	—	150	500	—	300	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.15	1.5	—	0.2	2.5	—	0.3	4.0	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	25	—	14	30	—	16	40	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V, 0V ≤ V_{CM} ≤ 3.5V	95	105	—	90	95	—	85	90	—	dB
		$V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	100	110	—	94	105	—	90	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and V− = 0V, V+ = 5V to 30V	—	4	6	—	6	10	—	10	32	μV/V
Large-Signal Voltage Gain	A_{VO}	V+ = +5V, V− = 0V, 1V ≤ V_O ≤ 3.5V	300	500	—	200	500	—	—	500	—	V/mV
		$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 25k\Omega$	1000	2000	—	800	2000	—	500	1000	—	
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 10k\Omega$	0.6/4.1	—	—	0.7/4.1	—	—	0.8/4.0	—	—	V
		$V_S = \pm 15V$, $R_L = 25k\Omega$	±14.1	—	—	±14.1	—	—	±14.0	—	—	
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	—	100	—	—	100	—	—	100	—	kHz
Slew Rate	SR	$V_S = \pm 15V$, $R_L = 25k\Omega$	—	0.05	—	—	0.05	—	—	0.05	—	V/μs
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	40	55	—	44	63	—	45	70	μA
		$V_S = \pm 15V$, No Load	—	55	80	—	57	85	—	60	95	

ANALOG DEVICES

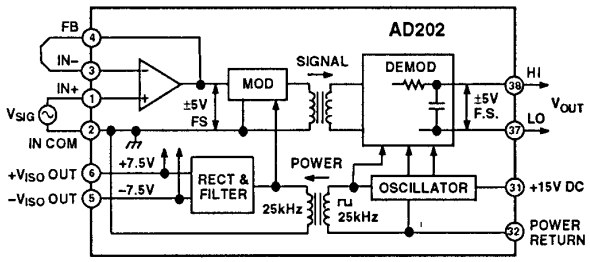
Low Cost, Miniature Isolation Amplifiers

AD202/AD204

FEATURES
Small Size: 4 Channels/Inch
Low Power: 35 mW (AD204)
High Accuracy: ±0.025% max Nonlinearity (K Grade)
High CMR: 130 dB (Gain = 100 V/V)
Wide Bandwidth: 5 kHz Full-Power (AD204)
High CMV Isolation: ±2000 V pk Continuous (K Grade) (Signal and Power)
Isolated Power Outputs
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
Current Shunt Measurements
Motor Controls
Process Signal Isolation
High Voltage Instrumentation Amplifier

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD202 and AD204 are general purpose, two-port, transformer-coupled isolation amplifiers that may be used in a broad range of applications where input signals must be measured, processed and/or transmitted without a galvanic connection. These industry standard isolation amplifiers offer a complete isolation function, with both signal and power isolation provided for in a single compact plastic SIP or DIP style package. The primary distinction between the AD202 and the AD204 is that the AD202 is powered directly from a +15 V dc supply while the AD204 is powered by an externally supplied clock, such as the recommended AD246 Clock Driver.

The AD202 and AD204 provide total galvanic isolation between the input and output stages of the isolation amplifier through the use of internal transformer-coupling. The functionally complete AD202 and AD204 eliminate the need for an external, user-supplied dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD202 and AD204 emphasizes maximum flexibility and ease of use, including the availability of an uncommitted op amp on the input stage. They feature a bipolar ±5 V output range, an adjustable gain range of from 1 to 100 V/V, ±0.025% max nonlinearity (K grade), 130 dB of CMR and the AD204 consumes a low 35 mW of power.

PRODUCT HIGHLIGHTS

The AD202 and AD204 are full-featured isolators offering numerous benefits to the user:

Small Size: The AD202 and AD204 are available in SIP and DIP form packages. The SIP package is just 0.25" wide, giving the user a channel density of four channels per inch. The isolation barrier is positioned to maximize input to output spacing. For applications requiring a low profile, the DIP package provides a height of just 0.350".

High Accuracy: With a maximum nonlinearity of ±0.025% for the AD202K/AD204K (±0.05% for the AD202J/AD204J) and low drift over temperature, the AD202 and AD204 provide high isolation without loss of signal integrity.

Low Power: Power consumption of 35 mW (AD204) and 75 mW (AD202) over the full signal range makes these isolators ideal for use in applications with large channel counts or tight power budgets.

Wide Bandwidth: The AD204's full-power bandwidth of 5 kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Excellent Common-Mode Performance: The AD202K/AD204K provide ±2000 V pk continuous common-mode isolation, while the AD202J/AD204J provide ±1000 V pk continuous common-mode isolation. All models have a total common-mode input capacitance of less than 5 pF inclusive of power isolation. This results in CMR ranging from 130 dB at a gain of 100 dB to 104 dB (minimum at unity gain) and very low leakage current (2 μA maximum).

Flexible Input: An uncommitted op amp is provided at the input of all models. This provides buffering and gain as required, and facilitates many alternative input functions including filtering, summing, high-voltage ranges, and current (transimpedance) input.

Isolated Power: The AD204 can supply isolated power of ±7.5 V at 2 mA. This is sufficient to operate a low-drift input preamp, provide excitation to a semiconductor strain gage, or to power any of a wide range of user-supplied ancillary circuits. The AD202 can supply ±7.5 V at 0.4 mA which is sufficient to operate adjustment networks or low-power references and op amps, or to provide an open-input alarm.

REV. B

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD202/AD204–SPECIFICATIONS (typical @ + 25°C & V_S = +15 V unless otherwise noted)

Model	AD204J	AD204K	AD202J	AD202K
GAIN				
Range	1 V/V–100 V/V	*	*	*
Error	±0.5% typ (±4% max)	*	*	*
vs. Temperature	±20 ppm/°C typ (±45 ppm/°C max)	*	*	*
vs. Time	±50 ppm/1000 Hours	*	*	*
vs. Supply Voltage	±0.01%/V	±0.01%/V	±0.01%/V	±0.01%/V
Nonlinearity (G = 1 V/V)[1]	±0.05% max	±0.025% max	±0.05% max	±0.025% max
Nonlinearity vs. Isolated Supply Load	±0.0015%/mA	*	*	*
INPUT VOLTAGE RATINGS				
Input Voltage Range	±5 V	*	*	*
Max Isolation Voltage (Input to Output)				
AC, 60 Hz, Continuous	750 V rms	1500 V rms	750 V rms	1500 V rms
Continuous (AC and DC)	±1000 V Peak	±2000 V Peak	±1000 V Peak	±2000 V Peak
Isolation-Mode Rejection Ratio (IMRR) @ 60 Hz				
$R_S \leq 100\ \Omega$ (HI & LO Inputs) G = 1 V/V	110 dB	110 dB	105 dB	105 dB
G = 100 V/V	130 dB	*	*	*
$R_S \leq 1\ k\Omega$ (Input HI, LO, or Both) G = 1 V/V	104 dB min	104 dB min	100 dB min	100 dB min
G = 100 V/V	110 dB min	*	*	*
Leakage Current Input to Output @ (240 V rms, 60 Hz	2 µA rms max	*	*	*'
INPUT IMPEDANCE				
Differential (G = 1 V/V)	$10^{12}\ \Omega$	*	*	*
Common Mode	2 GΩ‖4.5 pF	*	*	*
INPUT BIAS CURRENT				
Initial, @ +25°C	±30 pA	*	*	*
vs. Temperature (0°C to +70°C)	±10 nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±5 pA	*	*	*
vs. Temperature (0°C to +70°C)	±2 nA	*	*	*
INPUT NOISE				
Voltage, 0.1 Hz to 100 Hz	4 µV p-p	*	*	*
f > 200 Hz	50 nV/√Hz	*	*	*
FREQUENCY RESPONSE				
Bandwidth ($V_O \leq 10$ V p-p, G = 1 V–50 V/V)	5 kHz	5 kHz	2 kHz	2 kHz
Settling Time, to ±10 mV (10 V Step)	1 ms	*	*	*
OFFSET VOLTAGE (RTI)				
Initial, @ +25°C Adjustable to Zero	(±15 ±15/G)mV max	(±5 ±5/G)mVmax	(±15 ±15/G)mVmax	(±5 ±5/G)mVmax
vs . Temperature (0°C to +70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)\mu V/°C$			
RATED OUTPUT				
Voltage (Out HI to Out LO)	±5 V	*	*	*
Voltage at Out HI or Out LO (Ref. Pin 32)	±6.5 V	*	*	*
Output Resistance	3 kΩ	3 kΩ	7 kΩ	7 kΩ
Output Ripple, 100 kHz Bandwidth	10 mV pk-pk	*	*	*
5 kHz Bandwidth	0.5 mV rms	*	*	*
ISOLATED POWER OUTPUT[2]				
Voltage, No Load	±7.5 V	*	*	*
Accuracy	±10%	*	*	*
Current	2 mA (Either Output)[3]	2 mA (Either Output)[3]	400 µA Total	400 µA Total
Regulation, No Load to Full Load	5%	*	*	*
Ripple	100 mV pk-pk	*	*	*
OSCILLATOR DRIVE INPUT				
Input Voltage	15 V pk-pk Nominal	15 V pk-pk Nominal	N/A	N/A
Input Frequency	25 kHz Nominal	25 kHz Nominal	N/A	N/A
POWER SUPPLY (AD202 Only)				
Voltage, Rated Performance	N/A	N/A	+15 V ± 5%	+15 V ± 5%
Voltage, Operating	N/A	N/A	+15 V ± 10%	+15 V ± 10%
Current, No Load (V_S = +15 V)	N/A	N/A	5 mA	5 mA
TEMPERATURE RANGE				
Rated Performance	0°C to +70°C	*	*	*
Operating	–40°C to +85°C	*	*	*
Storage	–40°C to +85°C	*	*	*
PACKAGE DIMENSIONS[4]				
SIP Package (Y)	2.08" × 0.250" × 0.625"	*	*	*
DIP Package (N)	2.10" × 0.700" × 0.350"	*	*	*

NOTES
Specifications same as AD204J.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]1.0 µF min decoupling required (see text).
[3]3 mA with one supply loaded.
[4]Width is 0.25" typ, o.26" max.
Specifications subject to change without notice .

AD202/AD204

DIFFERENCES BETWEEN THE AD202 AND AD204

The primary distinction between the AD202 and AD204 is in the method by which they are powered: the AD202 operates directly from +15 V dc while the AD204 is powered by a non-isolated externally-supplied clock (AD246) which can drive up to 32 AD204s. The main advantages of using the externally-clocked AD204 over the AD202 are reduced cost in multichannel applications, lower power consumption, and higher bandwidth. In addition, the AD204 can supply substantially more isolated power than the AD202.

Of course, in a great many situations, especially where only one or a few isolators are used, the convenience of stand-alone operation provided by the AD202 will be more significant than any of the AD204's advantages. There may also be cases where it is desirable to accommodate either device interchangeably, so the pinouts of the two products have been designed to make that easy to do.

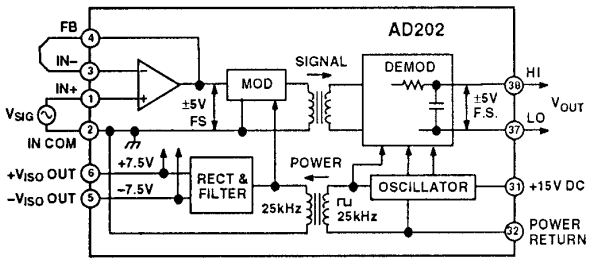


Figure 1a. AD202 Functional Block Diagram

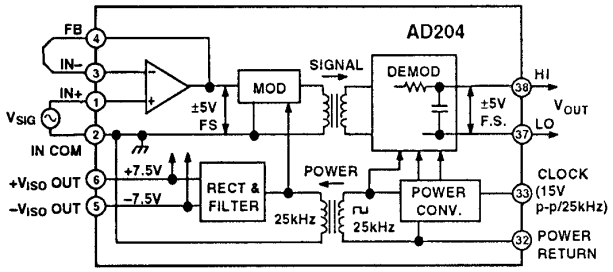


Figure 1b. AD204 Functional Block Diagram (Pin Designations Apply to the DIP-Style Package)

INSIDE THE AD202 AND AD204

The AD202 and AD204 use an amplitude modulation technique to permit transformer coupling of signals down to dc (Figure 1a and 1b). Both models also contain an uncommitted input op amp and a power transformer which provides isolated power to the op amp, the modulator, and any external load. The power transformer primary is driven by a 25 kHz, 15 V p-p square wave which is generated internally in the case of the AD202, or supplied externally for the AD204.

Within the signal swing limits of approximately ±5 V, the output voltage of the isolator is equal to the output voltage of the op amp; that is, the isolation barrier has unity gain. The output signal is not internally buffered, so the user is free to interchange the output leads to get signal inversion. Additionally, in multichannel applications, the unbuffered outputs can be multiplexed with one buffer following the mux. This technique minimizes offset errors while reducing power consumption and cost. The output resistance of the isolator is typically 3 kΩ for the AD204 (7 kΩ for AD202) and varies with signal level and temperature, so it should not be loaded (see Figure 2 for the effects of load upon nonlinearity and gain drift). In many cases a high-impedance load will be present or a following circuit such as an output filter can serve as a buffer, so that a separate buffer function will not often be needed.

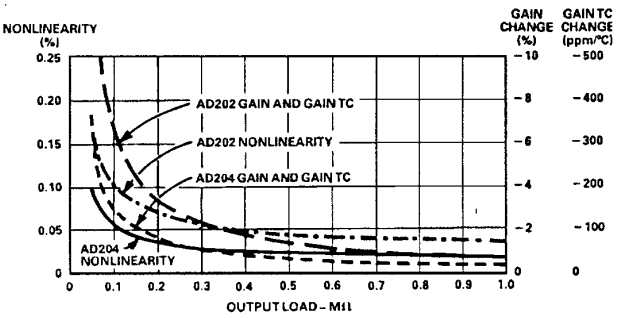


Figure 2. Effects of Output Loading

USING THE AD202 AND AD204

Powering the AD202. The AD202 requires only a single +15 V power supply connected as shown in Figure 3a. A bypass capacitor is provided in the module.

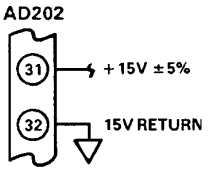


Figure 3a.

Powering the AD204. The AD204 gets its power from an externally supplied clock signal (a 15 V p-p square wave with a nominal frequency of 25 kHz) as shown in Figure 3b.

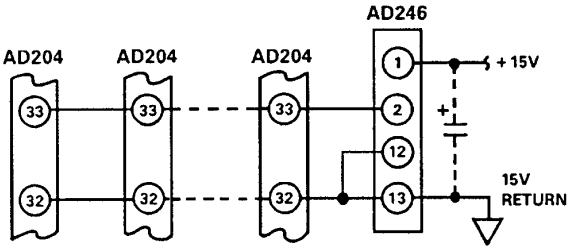


Figure 3b.

AD246 Clock Driver. The AD246 is a compact, inexpensive clock driver that can be used to obtain the required clock from a single 15 V supply. Alternatively, the circuit shown in Figure 4 (essentially an AD246) can be used. In either case, one clock circuit can operate at least 32 AD204s at the rated minimum supply voltage of 14.25 V and one additional isolator can be operated for each 40 mV increase in supply voltage up to 15 V. A supply bypass capacitor is included in the AD246, but if many

(Circuit figures shown on this page are for SIP style packages. Refer to page 3 for proper DIP package pinout.)

AD204s are operated from a single AD246, an external bypass capacitor should be used with a value of at least 1 µF for every five isolators used. Place the capacitor as close as possible to the clock driver.

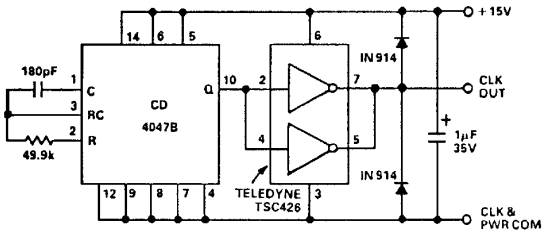


Figure 4. Clock Driver

Input Configurations. The AD202 and AD204 have been designed to be very easy to use in a wide range of applications. The basic connection for standard unity gain applications, useful for signals up to ±5 V, is shown in Figure 5; some of the possible variations are described below. When smaller signals must be

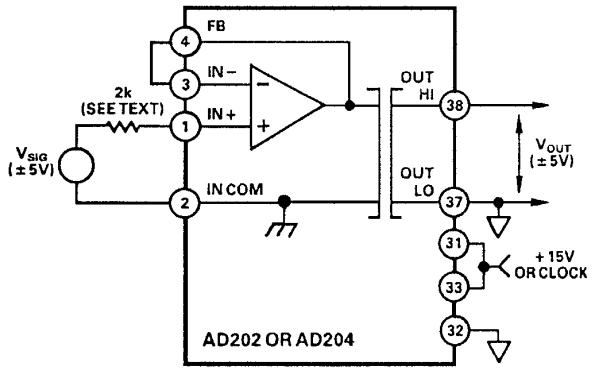


Figure 5. Basic Unity-Gain Application

handled, Figure 6 shows how to get gain while preserving a very high input resistance. The value of feedback resistor R_F should be kept above 20 kΩ for best results. Whenever a gain of more than five is taken, a 100 pF capacitor from FB to IN COM is required. At lower gains this capacitor is unnecessary, but it will not adversely affect performance if used.

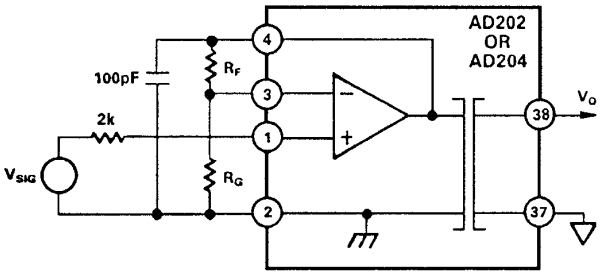


Figure 6. Input Connections for Gain > 1

The "noninverting" circuit of Figures 5 and 6 can also be used to advantage when a signal inversion is needed: just interchange either the input leads or the output leads to get inversion. This approach retains the high input resistance of the "noninverting" circuit, and at unity gain no gain-setting resistors are needed.

When the isolator is not powered, a negative input voltage of more than about 2 V will cause an input current to flow. If the signal source can supply more than a few mA under such conditions, the 2 kΩ resistor shown in series with IN+ should be used to limit current to a safe value. This is particularly important with the AD202, which may not start if a large input current is present.

Figure 7 shows how to accommodate current inputs or sum currents or voltages. This circuit can also be used when the input signal is larger than the ±5 V input range of the isolator; for example, a ±50 V input span can be accommodated with R_F = 20 k and R_S = 200 k. Once again, a capacitor from FB to IN COM is required for gains above five.

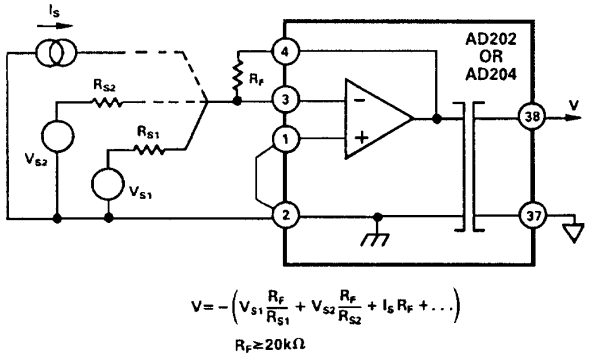


Figure 7. Connections for Summing or Current Inputs

Adjustments. When gain and zero adjustments are needed, the circuit details will depend on whether adjustments are to be made at the isolator input or output, and (for input adjustments) on the input circuit used. Adjustments are usually best done on the input side, because it is better to null the zero ahead of the gain, and because gain adjustment is most easily done as part of the gain-setting network. Input adjustments are also to be preferred when the pots will be near the input end of the isolator (to minimize common-mode strays). Adjustments on the output side might be used if pots on the input side would represent a hazard due to the presence of large common-mode voltages during adjustment.

Figure 8a shows the input-side adjustment connections for use with the "noninverting" connection of the input amplifier. The zero adjustment circuit injects a small adjustment voltage in series with the low side of the signal source. (This will not work if the source has another current path to input common or if current flows in the signal source LO lead). Since the adjustment voltage is injected ahead of the gain, the values shown will

(Circuit figures shown on this page are for SIP style packages. Refer to Page 3 for proper DIP package pinout.)

work for any gain. Keep the resistance in series with input LO below a few hundred ohms to avoid CMR degradation.

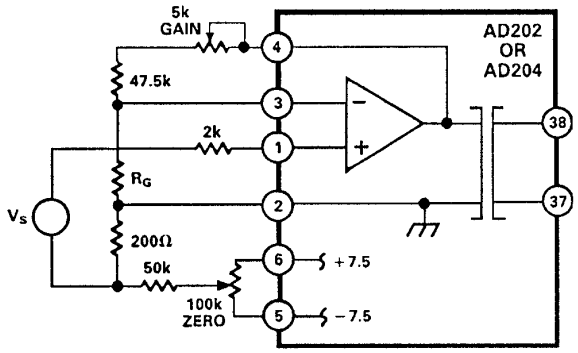


Figure 8a. Adjustments for Noninverting Connection of Op Amp

Also shown in Figure 8a is the preferred means of adjusting the gain-setting network. The circuit shown gives a nominal R_F of 50 kΩ, and will work properly for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input resistance; it is better to adjust gain at the signal source or after the output.

Figure 8b shows adjustments for use with inverting input circuits. The zero adjustment nulls the voltage at the summing node. This method is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is again done in the feedback; but in this case it will work all the way down to unity gain (and below) without alteration.

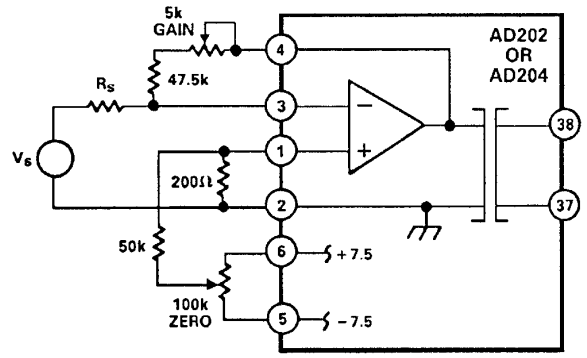


Figure 8b. Adjustments for Summing or Current Input

Figure 9 shows how zero adjustment is done at the output by taking advantage of the semi-floating output port. The range of this adjustment will have to be increased at higher gains; if that is done, be sure to use a suitably stable supply voltage for the pot circuit.

There is no easy way to adjust gain at the output side of the isolator itself. If gain adjustment must be done on the output side, it will have to be in a following circuit such as an output buffer or filter.

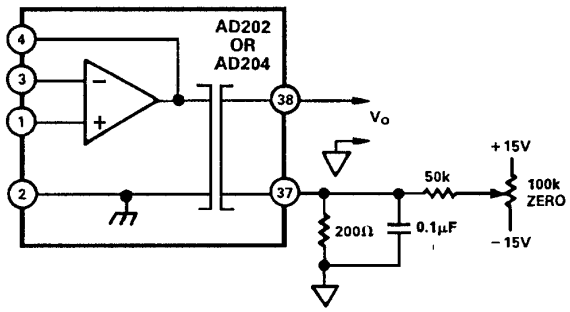


Figure 9. Output-Side Zero Adjustment

Common-Mode Performance. Figures 10a and 10b show how the common-mode rejection of the AD202 and AD204 varies with frequency, gain, and source resistance. For these isolators, the significant resistance will normally be that the path from the source of the common-mode signal to IN COM. The AD202 and AD204 also perform well in applications requiring rejection of fast common-mode steps, as described in the Applications section.

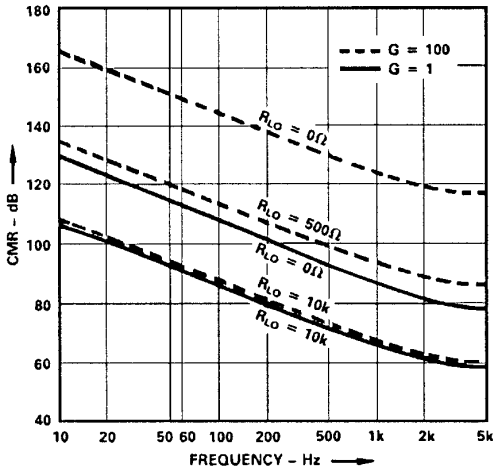


Figure 10a. AD204

(Circuit figures shown on this page are for SIP style packages. Refer to page 3 for proper DIP package pinout.)

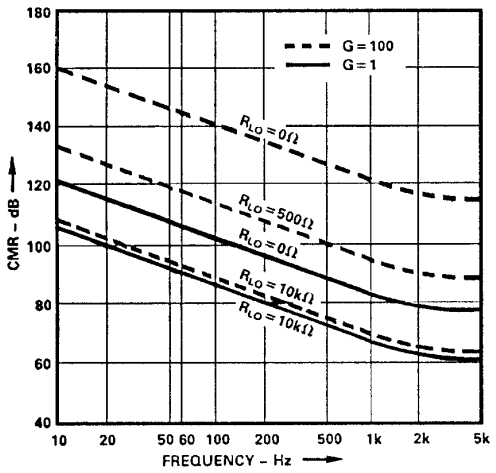


Figure 10b. AD202

Dynamics and Noise. Frequency response plots for the AD202 and AD204 are given in Figure 11. Since neither isolator is slew-rate limited, the plots apply for both large and small signals. Capacitive loads of up to 470 pF will not materially affect frequency response. When large signals beyond a few hundred Hz will be present, it is advisable to bypass $-V_{ISO}$ and $+V_{ISO}$ to IN COM with 1 µF tantalum capacitors even if the isolated supplies are not loaded.

At 50 Hz/60 Hz, phase shift through the AD202/AD204 is typically 0.8° (lagging). Typical unit—unit variation is ±0.2° (lagging).

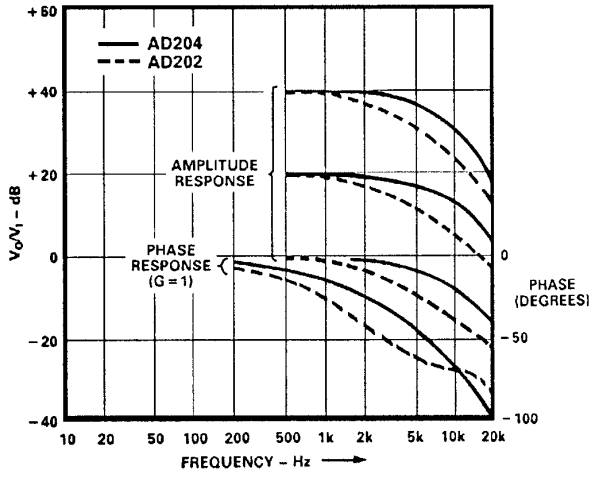


Figure 11. Frequency Response at Several Gains

The step response of the AD204 for very fast input signals can be improved by the use of an input filter, as shown in Figure 12. The filter limits the bandwidth of the input (to about 5.3 kHz) so that the isolator does not see fast, out-of-band input terms that can cause small amounts (±0.3%) of internal ringing. The AD204 will then settle to ±0.1% in about 300 microseconds for a 10 V step.

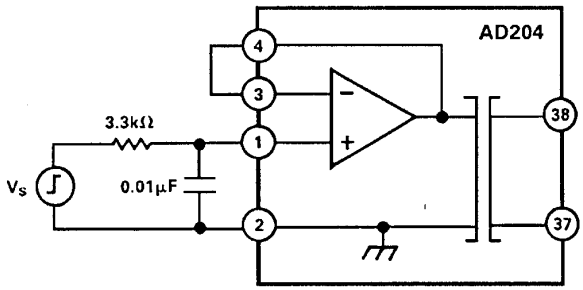


Figure 12. Input Filter for Improved Step Response

Except at the highest useful gains, the noise seen at the output of the AD202 and AD204 will be almost entirely comprised of carrier ripple at multiples of 25 kHz. The ripple is typically 2 mV p-p near zero output and increases to about 7 mV p-p for outputs of ±5 V (1 MHz measurement bandwidth). Adding a capacitor across the output will reduce ripple at the expense of bandwidth: for example, 0.05 µF at the output of the AD204 will result in 1.5 mV ripple at ±5 V, but signal bandwidth will be down to 1 kHz.

When the full isolator bandwidth is needed, the simple two-pole active filter shown in Figure 13 can be used. It will reduce ripple to 0.1 mV p-p with no loss of signal bandwidth, and also serves as an output buffer.

An output buffer or filter may sometimes show output spikes that do not appear at its input. This is usually due to clock noise appearing at the op amp's supply pins (since most op amps have little or no supply rejection at high frequencies). Another common source of carrier-related noise is the sharing of a ground track by both the output circuit and the power input. Figure 13 shows how to avoid these problems: the clock/supply port of the isolator does not share ground or 15 V tracks with any signal circuits, and the op amp's supply pins are bypassed to signal common (note that the grounded filter capacitor goes here as well). Ideally, the output signal LO lead and the supply common meet where the isolator output is actually measured, e.g., at an A/D converter input. If that point is more than a few feet from the isolator, it may be useful to bypass output LO to supply common at the isolator with a 0.1 µF capacitor.

In applications where more than a few AD204s are driven by a single clock driver, substantial current spikes will flow in the power return line and in whichever signal out lead returns to a low impedance point (usually output LO). Both of these tracks

(Circuit figures shown on this page are for SIP style packages. Refer to page 3 for proper DIP package pinout.)

should be made large to minimize inductance and resistance; ideally, output LO should be directly connected to a ground plane which serves as measurement common.

Current spikes can be greatly reduced by connecting a small inductance (68 µH–100 µH) in series with the clock pin of each AD204. Molded chokes such as the Dale IM-2 series, with dc resistance of about 5 Ω, are suitable.

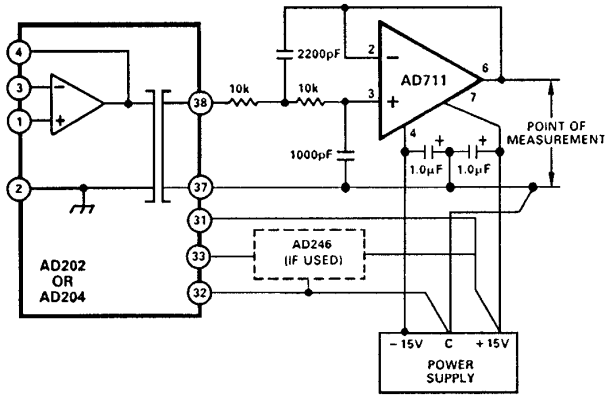


Figure 13. Output Filter Circuit Showing Proper Grounding

Using Isolated Power. Both the AD202 and the AD204 provide ±7.5 V power outputs referenced to input common. These may be used to power various accessory circuits which must operate at the input common-mode level; the input zero adjustment pots described above are an example, and several other possible uses are shown in the section titled Application Examples.

The isolated power output of the AD202 (400 µA total from either or both outputs) is much more limited in current capacity than that of the AD204, but it is sufficient for operating micropower op amps, low power references (such as the AD589), adjustment circuits, and the like.

The AD204 gets its power from an external clock driver, and can handle loads on its isolated supply outputs of 2 mA for each supply terminal (+7.5 V and –7.5 V) or 3 mA for a single loaded output. Whenever the external load on either supply is more than about 200 µA, a 1 µF tantalum capacitor should be used to bypass each loaded supply pin to input common.

Up to 32 AD204s can be driven from a single AD246 (or equivalent) clock driver when the isolated power outputs of the AD204s are loaded with less than 200 µA each, at a worst-case supply voltage of 14.25 V at the clock driver. The number of AD204s that can be driven by one clock driver is reduced by one AD204 per 3.5 mA of isolated power load current at 7.5 V, distributed in any way over the AD204s being supplied by that clock driver. Thus a load of 1.75 mA from $+V_{ISO}$ to $-V_{ISO}$ would also count as one isolator because it spans 15 V.

It is possible to increase clock fanout by increasing supply voltage above the 14.25 V minimum required for 32 loads. One additional isolator (or 3.5 mA unit load) can be driven for each 40 mV of increase in supply voltage up to 15 V. Therefore if the minimum supply voltage can be held to 15 V – 1%, it is possible to operate 32 AD204s and 52 mA of 7.5 V loads. Figure 14 shows the allowable combinations of load current and channel count for various supply voltages.

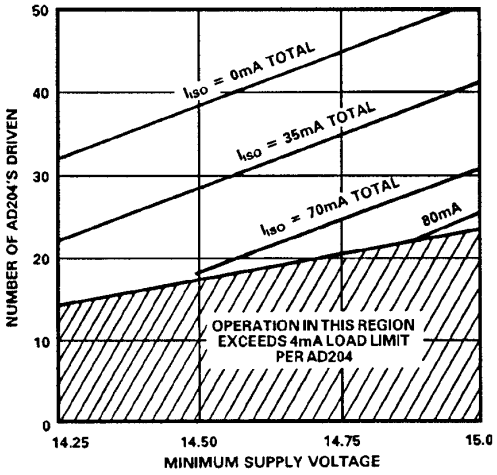


Figure 14. AD246 Fanout Rules

Synchronization. Since AD204s operate from a common clock, synchronization is inherent. AD202s will normally not interact to produce beat frequencies even when mounted on 0.25-inch centers. Interaction may occur in rare situations where a large number of long, unshielded input cables are bundled together and channel gains are high. In such cases, shielded cable may be required or AD204s can be used.

APPLICATIONS EXAMPLES

Low-Level Sensor Inputs. In applications where the output of low-level sensors such as thermocouples must be isolated, a low drift input amplifier can be used with an AD204, as shown in Figure 17. A three-pole active filter is included in the design to get normal-mode rejection of frequencies above a few Hz and to provide enhanced common-mode rejection at 60 Hz. If offset adjustment is needed, it is best done at the trim pins of the OP07 itself; gain adjustment can be done at the feedback resistor.

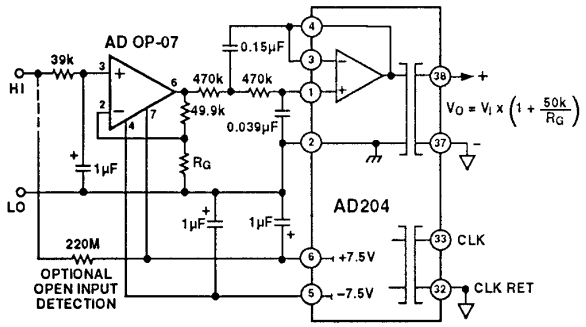


Figure 17. Input Amplifier & Filter for Sensor Signals

Note that the isolated supply current is large enough to mandate the use of 1 µF supply bypass capacitors. This circuit can be used with an AD202 if a low-power op amp is used instead of the OP07.

Process Current Input with Offset. Figure 18 shows an isolator receiver which translates a 4-20 mA process current signal into a 0 V to +10 V output. A 1 V to 5 V signal appears at the isolator's output, and a −1 V reference applied to output LO provides the necessary level shift (in multichannel applications, the reference can be shared by all channels). This technique is often useful for getting offset with a follower-type output buffer.

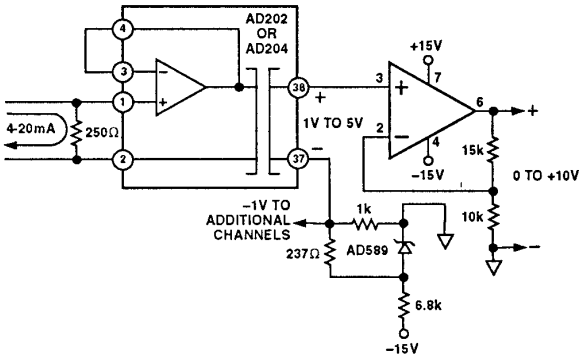


Figure 18. Process Current Input Isolator with Offset

The circuit as shown requires a source compliance of at least 5 V, but if necessary that can be reduced by using a lower value of current-sampling resistor and configuring the input amplifier for a small gain.

High-Compliance Current Source. In Figure 19, an isolator is used to sense the voltage across current-sensing resistor R to allow direct feedback control of a high-voltage transistor or FET used as a high-compliance current source. Since the isolator has virtually no response to dc common-mode voltage, the closed-loop current source has a static output resistance greater than 10^{14} Ω even for output currents of several mA. The output current capability of the circuit is limited only by power dissipation in the source transistor.

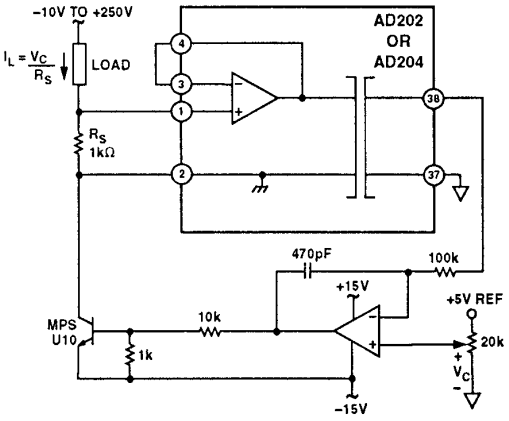


Figure 19. High-Compliance Current Source

PMI

OP-77

NEXT GENERATION OP-07
(ULTRA-LOW OFFSET VOLTAGE OPERATIONAL AMPLIFIER)

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Outstanding Gain Linearity
- Ultra High Gain ..... 5000V/mV Min
- Low V_{OS} ..... 25μV Max
- Excellent TCV_{OS} ..... 0.3μV/°C Max
- High PSRR ..... 3μV/V Max
- High CMRR ..... 1.0μV/V Max
- Low Power Consumption ..... 60mW Max
- Fits OP-07, 725, 108A/308A, 741 Sockets

ORDERING INFORMATION†

PACKAGE			
TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
OP77AJ*	OP77AZ*		MIL
OP77EJ	OP77EZ	OP77EP	IND
OP77BJ*	OP77BZ*		MIL
OP77FJ	OP77FZ	OP77FP	IND
	OP77GZ	OP77GP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-77 significantly advances the state-of-the-art in precision op amps. The OP-77's outstanding gain of 10,000,000 or more is maintained over the full ±10V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides superior performance in high closed-loop-gain applications.

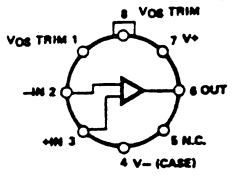
Low initial V_{OS} drift and rapid stabilization time, combined with only 50mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCV_{OS} of 0.3μV/°C maximum and the low V_{OS} of 25μV maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

PSRR of 3μV/V (110dB) and CMRR of 1.0μV/V maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP-77 ideally suited for high-resolution instrumentation and other tight error budget systems.

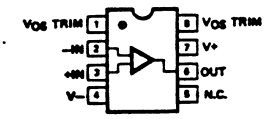
This product is available in five standard grades and three standard packages: the TO-99 can and the 8-pin mini-dip in ceramic or epoxy.

The OP-77 is a direct or upgrade replacement for the OP-07, OP-05, 725, or 108A op amps. 741-types can be replaced by eliminating the V_{OS} adjust pot.

PIN CONNECTIONS

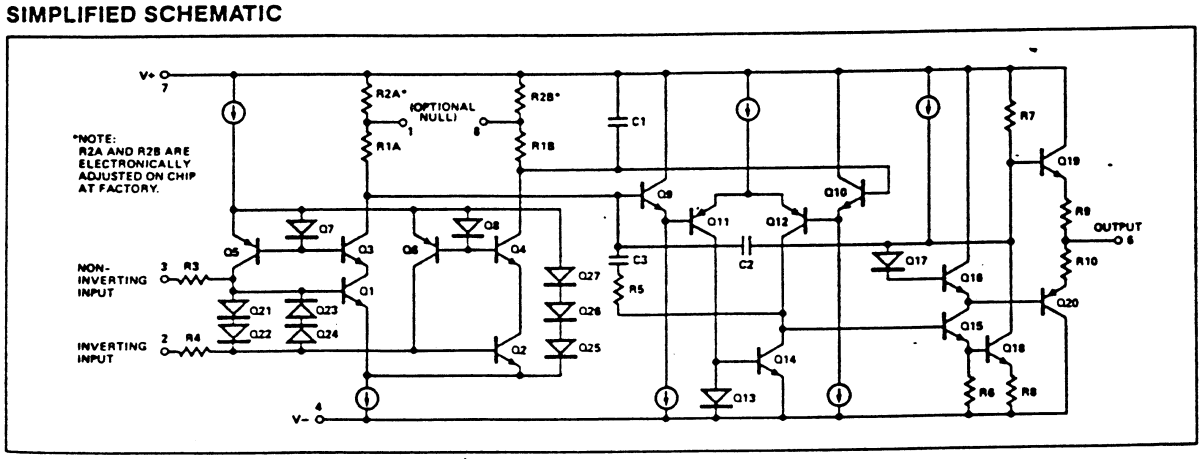


TO-99 (J-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 3) ..... ±22V
Output Short-Circuit Duration .....Indefinite
Storage Temperature Range
J and Z Packages ..... −65°C to +150°C
P Package ..... −65°C to +125°C
Operating Temperature Range
OP-77A, OP-77B ..... −55°C to +125°C
OP-77E, OP-77F ..... −25°C to +85°C
OP-77G ..... 0°C to 70°C
Lead Temperature Range (Soldering, 60 sec).....300°C
DICE Junction Temperature (T_J) ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A MIN	OP-77A TYP	OP-77A MAX	OP-77B MIN	OP-77B TYP	OP-77B MAX	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	20	60	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	—	0.2	—	—	0.2	—	µV/Mo
Input Offset Current	I_{OS}		—	0.1	1.5	—	0.1	2.8	nA
Input Bias Current	I_B		−0.2	1.2	2.0	−0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2)	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		f_O = 100Hz (Note 2)	—	10.0	13.0	—	10.0	13.0	
		f_O = 1000Hz (Note 2)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz (Note 2)	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		f_O = 100Hz (Note 2)	—	0.14	0.23	—	0.14	0.23	
		f_O = 1000Hz (Note 2)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	26	45	—	18.5	45	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	—	0.1	1.0	—	0.1	1.6	µV/V
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	—	1.0	3	—	1.0	3	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	5000	12000	—	2000	8000	—	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ	±13.5	±14.0	—	±13.5	±14.0	—	V
		R_L ≥ 2kΩ	±12.5	±13.0	—	±12.5	±13.0	—	
		R_L ≥ 1kΩ	±12.0	±12.5	—	±12.0	±12.5	—	
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	—	0.1	0.3	—	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	60	—	—	60	—	Ω
Power Consumption	P_d	V_S = ±15V, No Load	—	50	60	—	50	60	mW
		V_S = ±3V, No Load	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		R_P = 20kΩ	—	±3	—	—	±3	—	mV

NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV.
2. Sample tested.
3. Guaranteed by design.

LM111, LM211, LM311, LM311Y
DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007A – SEPTEMBER 1973 – REVISED FEBRUARY 1992

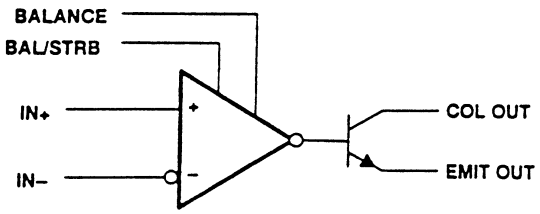
- **Fast Response Times**
- **Strobe Capability**
- **Maximum Input Bias Current . . . 300 nA**
- **Maximum Input Offset Current . . . 70 nA**
- **Can Operate From Single 5-V Supply**
- **Designed to Be Interchangeable With National Semiconductor LM111, LM211, and LM311**

description

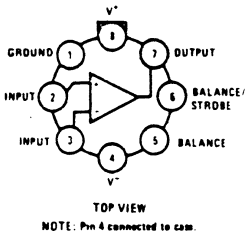
The LM111, LM211, and LM311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power supply voltages, including ±15-V supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+} or V_{CC-}. Offset balancing and strobe capabilities are available, and the outputs can be wire-OR connected. If the strobe is low, the output will be in the off state regardless of the differential input.

The LM111 is characterized for operation over the full military range of −55°C to 125°C. The LM211 is characterized for operation from −40°C to 85°C, and the LM311 is characterized for operation from 0°C to 70°C.

functional block diagram

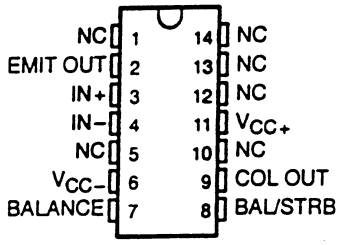


Metal Can Package

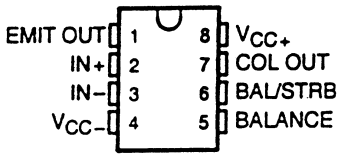


NOTE: Pin 4 connected to case.

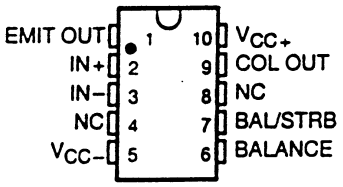
LM111 . . . J PACKAGE
(TOP VIEW)



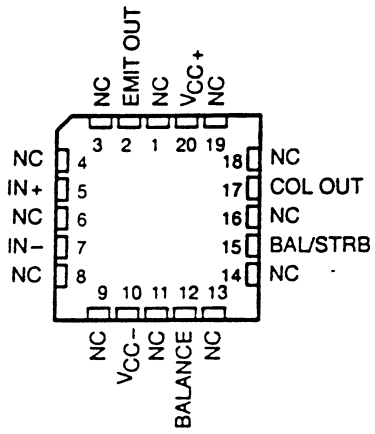
LM111 . . . JG PACKAGE
LM211, LM311 . . . D, DB, P, OR PW PACKAGE
(TOP VIEW)



LM111 . . . U PACKAGE
(TOP VIEW)



LM111 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

LM111, LM211, LM311, LM311Y
DIFFERENTIAL COMPARATORS WITH STROBES

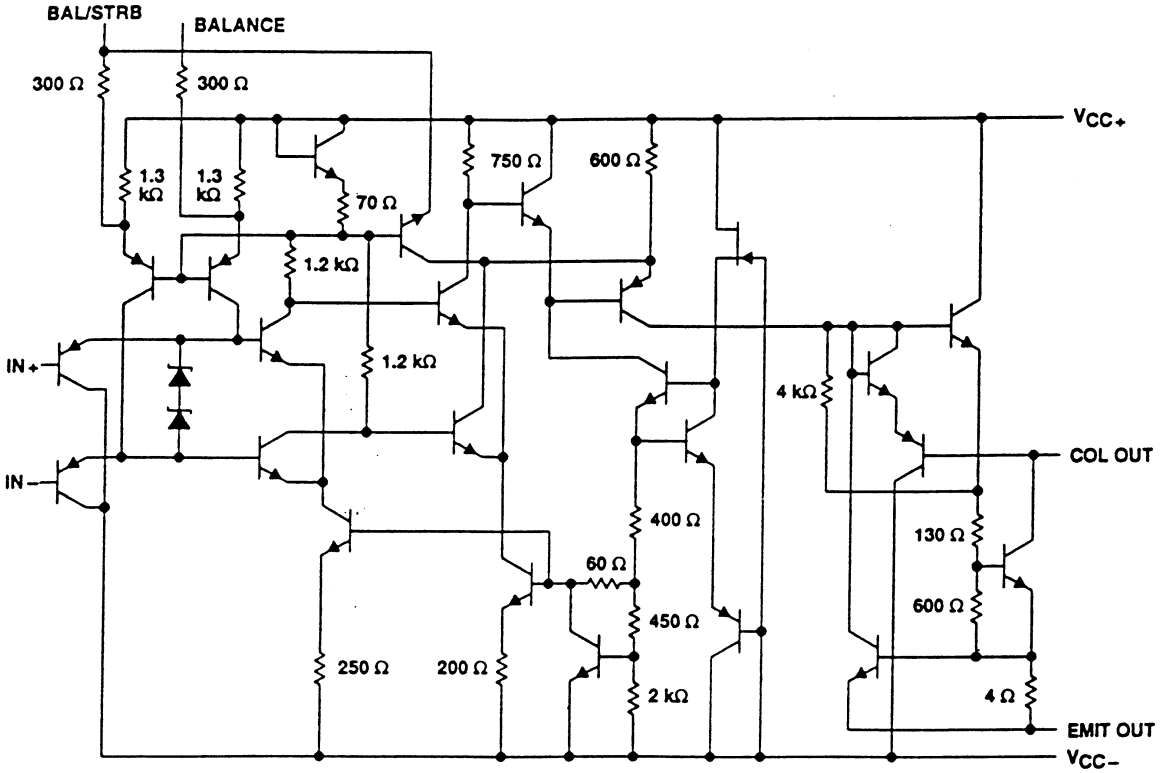
SLCS007A – SEPTEMBER 1973 – REVISED FEBRUARY 1992

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGED DEVICES								CHIP FORM (Y)
		SMALL OUTLINE (D)†	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	FLATPACK (U)	
0°C to 70°C	7.5 mV	LM311D	LM311DBLE				LM311P	LM311PWLE		LM311Y
−40°C to 85°C	3 mV	LM211D					LM211P			
−55°C to 125°C	3 mV			LM111FK	LM111J	LM111JG			LM111U	

† The D package is available taped and reeled. Add the suffix R (e.g., LM311DR). The DB and PW packages are only available left-end taped and reeled.

schematic



Component Count	
Resistors	20
Diodes	2
Epifet	1
Transistors	22

All resistor values shown are nominal.

LM111, LM211, LM311, LM311Y
DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007A – SEPTEMBER 1973 – REVISED FEBRUARY 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 18 V
Supply voltage, V_{CC-} (see Note 1) ..... −18 V
Supply voltage, $V_{CC+} - V_{CC-}$ ..... 36 V
Differential input voltage, V_{ID} (see Note 2) ..... ±30 V
Input voltage, V_I (either input, see Notes 1 and 3) ..... ±15 V
Voltage from emitter output to V_{CC-} ..... 30 V
Voltage from collector output to V_{CC-}: LM111 ..... 50 V
LM211 ..... 50 V
LM311 ..... 40 V
Duration of output short circuit (see Note 4) ..... 10 s
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: LM111 ..... −55°C to 125°C
LM211 ..... −40°C to 85°C
LM311 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or U package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, DB, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 V, whichever is less.
4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	–
DB or PW	500 mW	4.2 mW/°C	31°C	336 mW	–	–
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	–
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC+} - V_{CC-}$		3.5	30	V
Input voltage ($\lvert V_{CC\pm}\rvert \le 15$ V)		$V_{CC-} + 0.5$	$V_{CC+} - 1.5$	V
Operating free-air temperature range, T_A	LM111	−55	125	°C
	LM211	−40	85	
	LM311	0	70	

National Semiconductor

February 1988

CD4020BM/CD4020BC
14-Stage Ripple Carry Binary Counters
CD4040BM/CD4040BC
12-Stage Ripple Carry Binary Counters
CD4060BM/CD4060BC
14-Stage Ripple Carry Binary Counters

CD4020BM/BC 14-Stage Ripple Carry Binary Counters/CD4040BM/BC 12-Stage Ripple Carry Binary Counters CD4060BM/BC 14-Stage Ripple Carry Binary Counters

General Description

The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

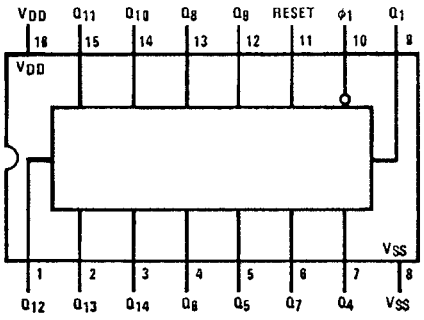
Features

■ Wide supply voltage range	1.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8 MHz typ. at V_{DD} = 10V
■ Schmitt trigger clock input	

Connection Diagrams

Dual-In-Line Package

CD4020BM/CD4020BC



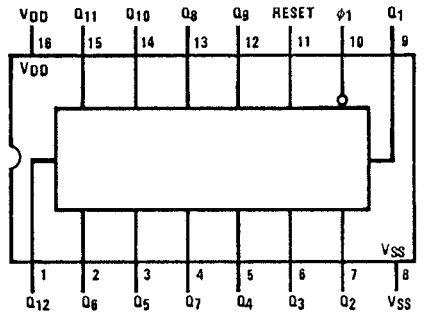
TL/F/5953–1

Top View

Order Number CD4020B, CD4040B or CD4060B

Dual-In-Line Package

CD4040BM/CD4040BC

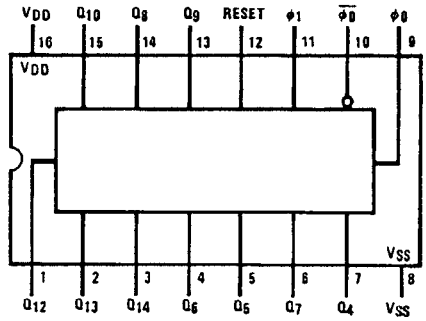


TL/F/5953–2

Top View

Dual-In-Line Package

CD4060BM/CD4060BC



TL/F/5953–3

Top View

RRD-B30M105/Printed in U. S. A.

AC Electrical Characteristics* CD4060BM/CD4060BC

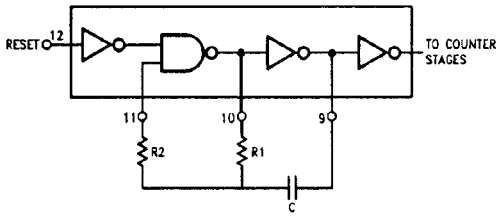
T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r = t_f = 20 ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	V_{DD} = 5V		550	1300	ns
		V_{DD} = 10V		250	525	ns
		V_{DD} = 15V		200	400	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	V_{DD} = 5V		150	330	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		45	90	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		170	500	ns
		V_{DD} = 10V		65	170	ns
		V_{DD} = 15V		50	125	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			No Limit	ns
		V_{DD} = 10V			No Limit	ns
		V_{DD} = 15V			No Limit	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1	3		MHz
		V_{DD} = 10V	3	8		MHz
		V_{DD} = 15V	4	10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
C_{in}	Average Input Capacitance	Any Input		5	7.5	pF
C_{pd}	Power Dissipation Capacitance			50		pF

*AC Parameters are guaranteed by DC correlated testing.

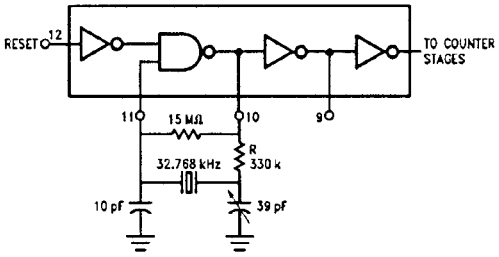
CD4060B Typical Oscillator Connections

RC Oscillator



TL/F/5953–4

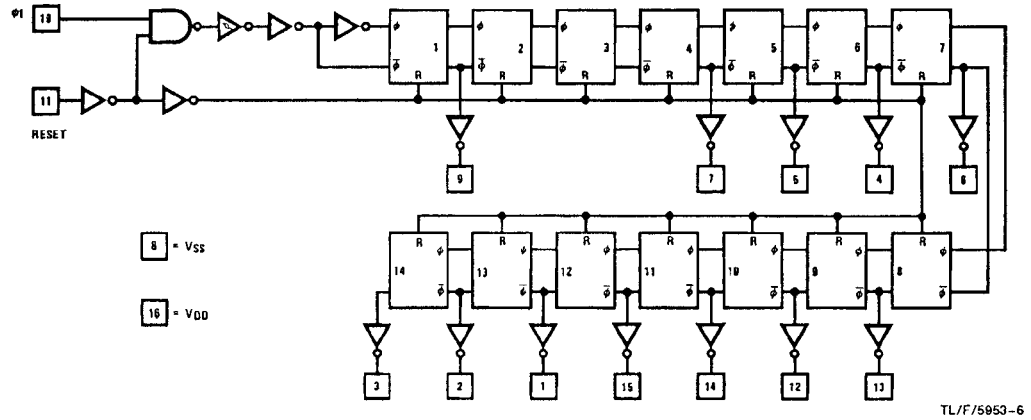
Crystal Oscillator



TL/F/5953–5

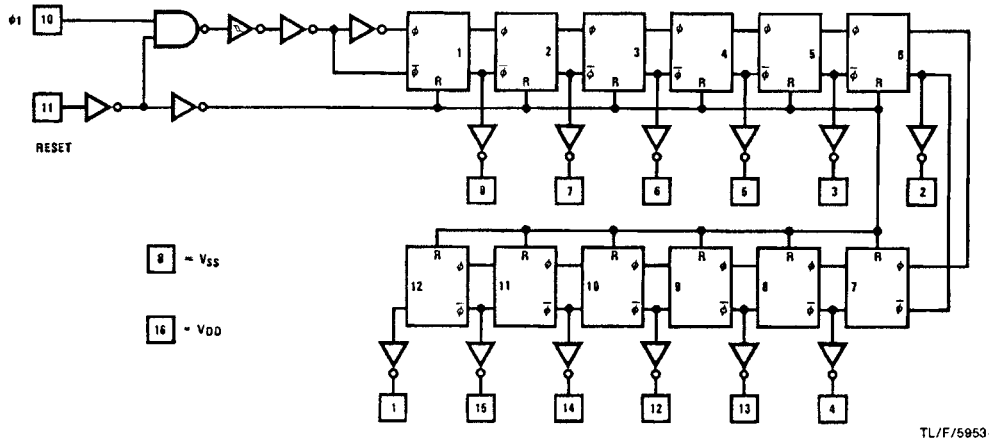
Schematic Diagrams

CD4020BM/CD4020BC Schematic Diagram



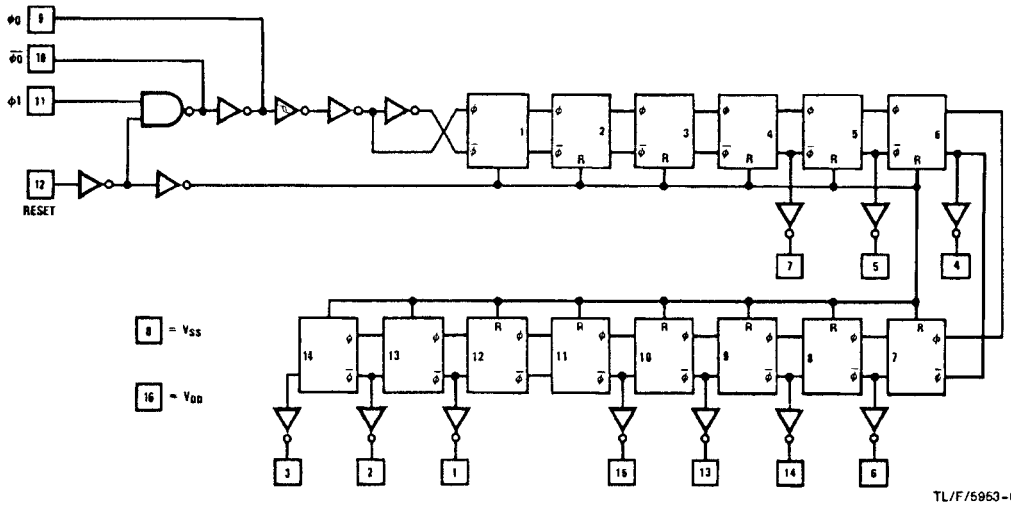
TL/F/5953–6

CD4040BM/CD4040BC Schematic Diagram



TL/F/5953–7

CD4060BM/CD4060BC Schematic Diagram



TL/F/5953–8

LINEAR TECHNOLOGY

LTC1061

High Performance Triple Universal Filter Building Block

FEATURES

- Up to 6th Order Filter Functions with a Single 20-Pin 0.3" Wide Package
- Center Frequency Range up to 35kHz
- $f_0 \times Q$ Product up to 1MHz
- *Guaranteed* Center Frequency and Q Accuracy Over Temperature
- *Guaranteed* Low Offset Voltages Over Temperature
- 90dB Signal-to-Noise Ratio
- Filter Operates from Single 4.7V Supply and up to ±8V Supplies
- *Guaranteed* Filter Specifications with ±5V Supply and ±2.37V Supply
- Low Power Consumption with Single 5V Supply
- Clock Inputs T^2L and CMOS Compatible

APPLICATIONS

- High Order, Wide Frequency Range Bandpass, Lowpass, Notch Filters
- Low Power Consumption, Single 5V Supply, Clock-Tunable Filters
- Tracking Filters
- Antialiasing Filters

LTCMOS™ is a trademark of Linear Technology Corp.

DESCRIPTION

The LTC1061 consists of three high performance, universal filter building blocks. Each filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce highpass or notch or allpass. The center frequency of these functions can be tuned with an external clock or an external clock and a resistor ratio. For $Q < 5$, the center frequency ranges from 0.1Hz to 35kHz. For Qs of 10 or above, the center frequency ranges from 0.1Hz to 28kHz.

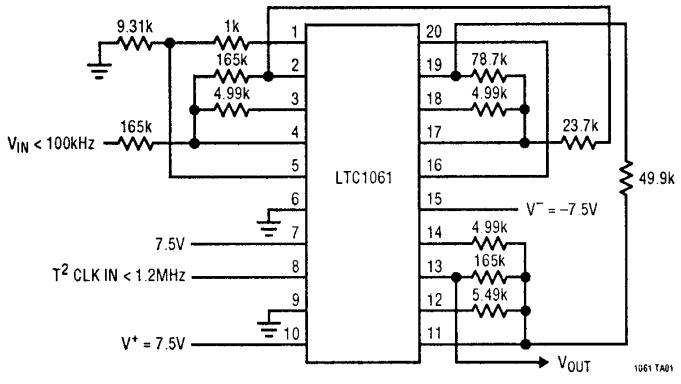
The LTC1061 can be used with single or dual supplies ranging from ±2.37V to ±8V (or 4.74V to 16V). When the filter operates with supplies of ±5V and above, it can handle input frequencies up to 100kHz.

The LTC1061 is compatible with the LTC1059 single universal filter and the LTC1060 dual. Higher than 6th order functions can be obtained by cascading the LTC1061 with the LTC1059 or LTC1060. Any classical filter realization can be obtained.

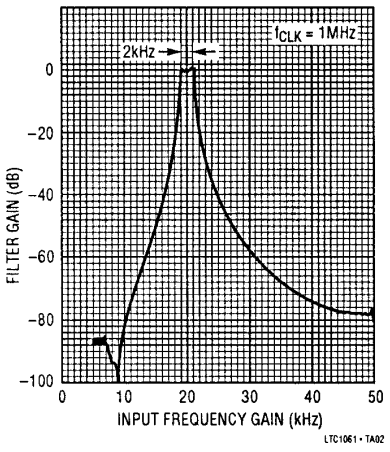
The LTC1061 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

TYPICAL APPLICATION

6th Order, Clock-Tunable, 0.5dB Ripple Chebyshev BP Filter



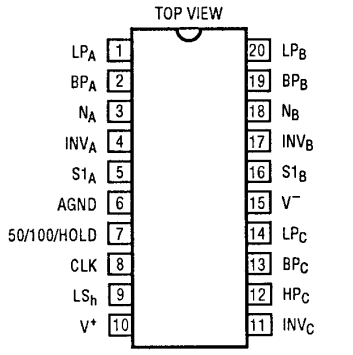
Amplitude Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Power Dissipation 500mW
Operating Temperature Range
LTC1061AC, LTC1061C ..... $-40°C \le T_A \le 85°C$
LTC1061AM, LTC1061M ..... $-55°C \le T_A \le 125°C$
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
20-LEAD CERAMIC DIP

N PACKAGE
20-LEAD PLASTIC DIP

S PACKAGE
20-LEAD PLASTIC SOL

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 100°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 100°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LTC1061AMJ
LTC1061MJ
LTC1061ACJ
LTC1061CJ
LTC1061ACN
LTC1061CN
LTC1061CS

Consult factory for Industrial grade parts

ELECTRICAL CHARACTERISTICS

(Complete Filter)V_S = ±5V, T_A = 25°C, T^2L clock input level, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_O	$f_O \times Q \le 175kHz$, Mode 1, V_S = ±7.5V			0.1–35k		Hz
	$f_O \times Q \le 1.6MHz$, Mode 1, V_S = ±7.5V			0.1–25k		Hz
	$f_O \times Q \le 75kHz$, Mode 3, V_S = ±7.5V			0.1–25k		Hz
	$f_O \times Q \le 1MHz$, Mode 3, V_S = ±7.5V			0.1–17k		Hz
Input Frequency Range				0–200k		Hz
Clock-to-Center Frequency Ratio, f_{CLK}/f_O	Sides A, B: Mode 1, R1 = R3 = 50k					
LTC1061A	R2 = 5k, Q = 10, f_{CLK} = 250kHz	●			50±0.6%	
LTC1061	Pin 7 High.	●			50±1.2%	
	Side C: Mode 3, R1 = R3 = 50k					
	R2 = R4 = 5k, f_{CLK} = 250kHz					
LTC1061A	Same as Above, Pin 7 at	●			100±0.6%	
LTC1061	Mid-Supplies, f_{CLK} = 500kHz	●			100±1.2%	
Clock-to-Center Frequency Ratio, Side-to-Side Matching						
LTC1061					1.2%	
Q Accuracy	Sides A, B, Mode 1					
LTC1061A	Side C, Mode 3	●		±2	5	%
LTC1061	$f_O \times Q \le 50kHz$, $f_O \times \le 5kHz$	●		±3	5	%
f_O Temperature Coefficient	Mode 1, 50:1, f_{CLK} < 300kHz			±1		ppm/°C
Q Temperature Coefficient	Mode 1, 100:1, f_{CLK} < 500kHz			±5		ppm/°C
	Mode 3, f_{CLK} < 500kHz			±5		ppm/°C

ELECTRICAL CHARACTERISTICS

(Complete Filter)V_S = ±5V, T_A = 25°C, T^2L clock input level, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Offset Voltage						
V_{OS1}, Figure 23		●		2	15	mV
V_{OS2}	f_{CLK} = 250kHz, 50:1	●		3	30	mV
V_{OS2}	f_{CLK} = 500kHz, 100:1	●		6	60	mV
V_{OS3}, LTC1061CN, ACN/LTC1061CS	f_{CLK} = 250kHz, 50:1	●		3	20/25	mV
V_{OS3}, LTC1061CN, ACN/LTC1061CS	f_{CLK} = 500kHz, 100:1	●		6	40/50	mV
Clock Feedthrough	f_{CLK} < 1MHz			0.4		mV_{RMS}
Maximum Clock Frequency	Mode 1, Q < 5, $V_S \geq \pm 5$			2.5		MHz
Power Supply Current			6	8	11	mA
		●			15	mA

(Complete Filter)V_S = ±2.37V, T_A = 25°C, unless otherwise specified.

Center Frequency Range, f_O	$f_O \times Q \leq$ 120kHz, Mode 1, 50:1			0.1–12k		Hz
	$f_O \times Q \leq$ 120kHz, Mode 3, 50:1			0.1–10k		Hz
Input Frequency Range				0–20k		Hz
Clock-to-Center Frequency Ratio	50:1, f_{CLK} = 250kHz, Q = 10					
LTC1061A	Sides A, B: Mode 1			50±0.6%		
LTC1061	Side C, Mode 3, 250kHz			50±1.0%		
LT1061A	100:1, f_{CLK} = 500kHz, Q = 10			100±0.6%		
LT1061	Sides A, B: Mode 1			100±1.0%		
	Side C: Mode 3					
Q Accuracy						
LTC1061A	Same as Above			±2		%
LTC1061				±3		%
Maximum Clock Frequency				700		kHz
Power Supply Current				4.5	6	mA

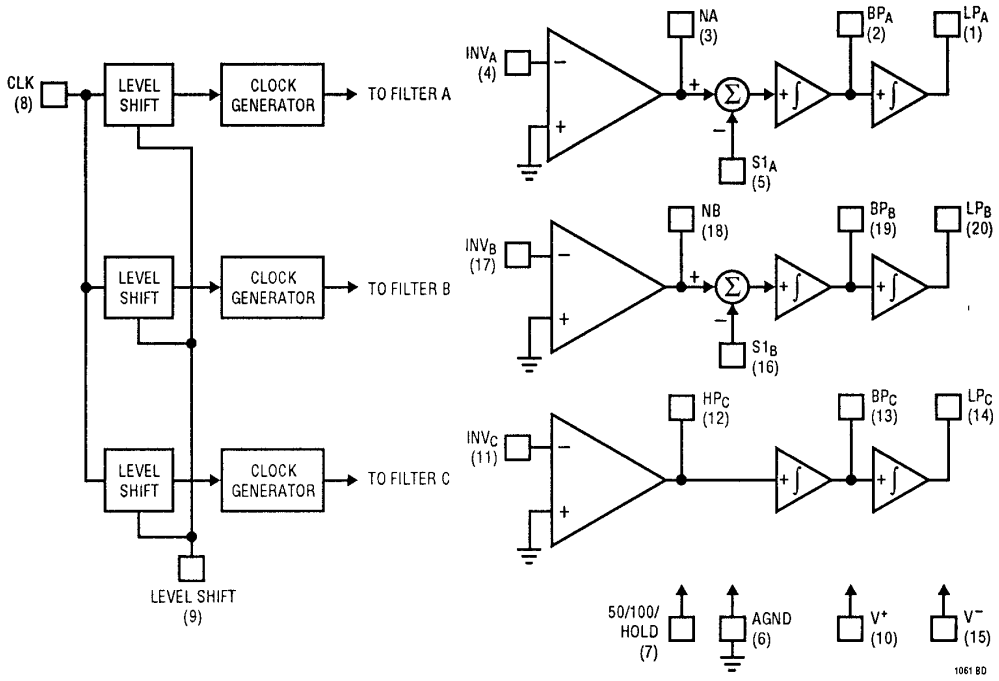
(Internal Op Amps) T_A = 25°C, unless otherwise specified.

Supply Voltage Range			±2.37		±9	V
Voltage Swings						
LTC1061A	V_S = ±5V, R_L = 5k (Pins 1,2,13,14,19,20)		±4.0	±4.2		V
LTC1061	V_S = ±5V, R_L = 3.5k (Pins 3,12,18)		±3.8	±4.2		V
LTC1061, LTC1061A		●	±3.6			V
Output Short-Circuit Current						
Source/Sink	V_S = ±5V			40/3		mA
DC Open-Loop Gain	V_S = ±5V, R_L = 5k			80		dB
GBW Product	V_S = ±5V			3		MHz
Slew Rate	V_S = ±5V			7		V/µs

The ● denotes the specifications which apply over the full operating temperature range.

Tournez la page S.V.P.

BLOCK DIAGRAM



PIN DESCRIPTION AND APPLICATION HINTS

Power Supplies (Pins 10, 15)

They should be bypassed with 0.1µF disc ceramic. Low noise, nonswitching, power supplies are recommended. The device operates with a single 5V supply, Figure 1, and with dual supplies. The absolute maximum operating power supply voltage is ±9V.

Clock and Level shift (Pins 8, 9)

When the LTC1061 operates with symmetrical dual supplies the level shift Pin 9 should be tied to analog ground. For single 5V supply operation, the level shift pin should be tied to Pin 15 which will be the system ground. The typical logic threshold levels of the clock pin are as follows: 1.65V above the level shift pin for ±5V supply operation, 1.75V for ±7.5V and above, and 1.4V for single 5V supply operation. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 300ns. The maximum clock frequency for ±5V supplies and above is 2.4MHz.

$S1_A$, $S1_B$ (Pins 5, 16)

These are voltage input pins. If used, they should be driven with a source impedance below 5kΩ. when they are not used, they should be tied to the analog ground Pin 6.

AGND (Pin 6)

When the LTC1061 operates with dual supplies, Pin 6 should be tied to system ground. When the LTC1061 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply, Figure 1. The positive input of all the internal op amps, as well as the common reference of all the internal switches, are internally tied to the analog ground pin. Because of this, a "clean" ground is recommended.

Tournez la page S.V.P.

PIN DESCRIPTION AND APPLICATION HINTS

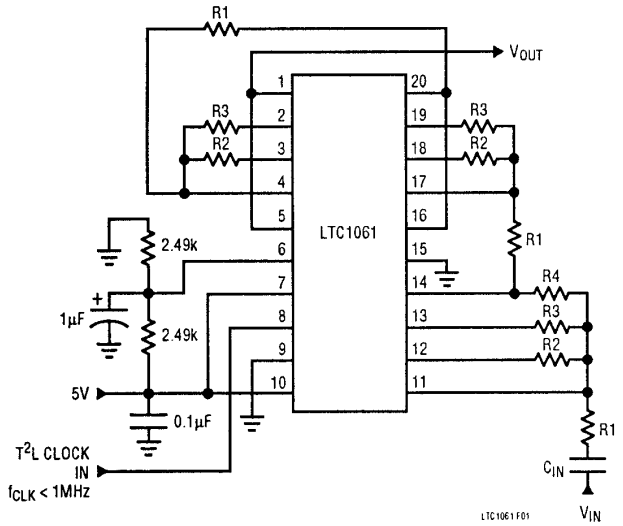


Figure 1. the 6th Order LP Butterworth Filter of Figure 5 Operating with a Single 5V Supply.

50/100/Hold (Pin 7)

By tying Pin 7 to V⁺, the filter operates with a clock-to-center frequency internally set at 50:1. When Pin 7 is at mid-supplies, the filter operates with a 100:1 clock-to-center frequency ratio. Table 1 shows the allowable variation of the potential at Pin 7 when the 100:1 mode is sought.

When Pin 7 is shorted to the negative supply pin, the filter operation is stopped and the bandpass and lowpass output act as a sample-and-hold circuit holding the last sample of the input voltage. The hold step is around 2mV and the droop rate is 150µV/sec.

Table 1

TOTAL POWER SUPPLY (V)	VOLTAGE RANGE OF PIN 7 FOR 100:1 OPERATION (V)
5	2.5 ± 0.5
10	5 ±1
15	7.5 ±1.5

Clock Feedthrough

This is defined as the amplitude of the clock frequency appearing at the output pins of the device, Figure 2. Clock feedthrough is measured with all three sides of the LTC1061 connected as filters. The clock feedthrough mainly depends on the magnitude of the power supplies and it is independent from the input clock levels, clock frequency and modes of operation.

The Table 2 illustrates the typical clock feedthrough numbers for various power supplies.

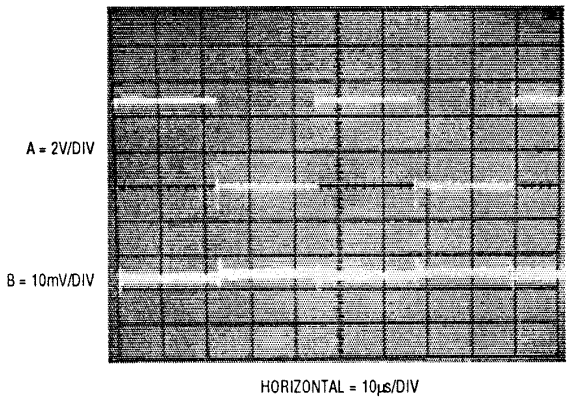


Figure 2. Typical Clock Feedthrogh of the LTC1061 Operating with ±5V Supplies. Top Trace is the Input Clock Swinging 0V to 5V and Bottom Trace is One of the Lowpass Outputs with Zero or DC Input Signals.

Table 2

POWER SUPPLY (V)	CLOCK FEEDTHROUGH (V_{RMS})
±2.5	0.2
±5	0.4
±8	0.8

Definition of Filter Functions

Refer to LTC1060 data sheet.

MODES OF OPERATION

Description and Applications

1. Primary Modes: There are two basic modes of operation, Mode 1 and Mode 3. In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at 50:1 or 100:1. In Mode 3, this ratio can be adjusted above or below 50:1 or 100:1. The side C of the LTC1061 can be connected only in Mode 3. Figure 3 illustrates Mode 1 providing 2nd order notch, lowpass, and bandpass outputs (for definition of filter functions, refer to the LTC1060 data sheet). Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency and with unity-gain. Mode 3, Figure 4, is the classical state variable configuration providing highpass, bandpass and lowpass 2nd order filter functions.

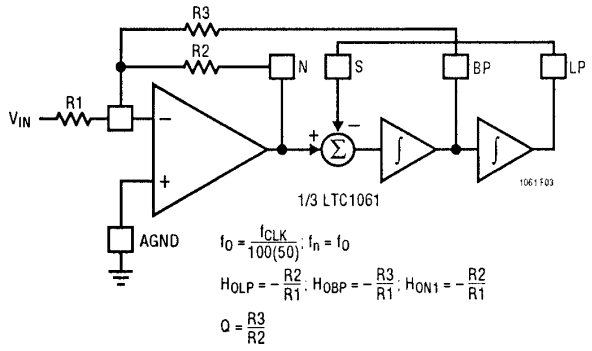


Figure 3. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

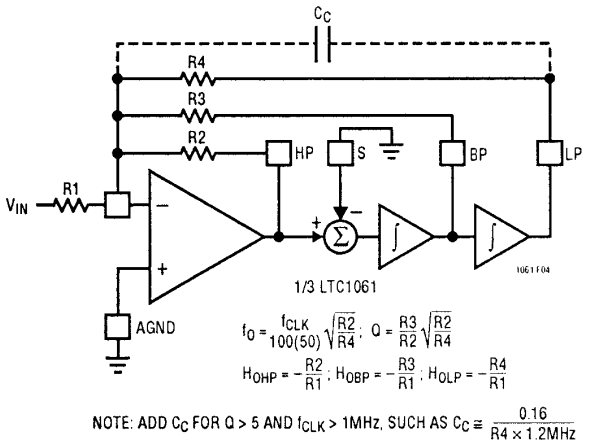
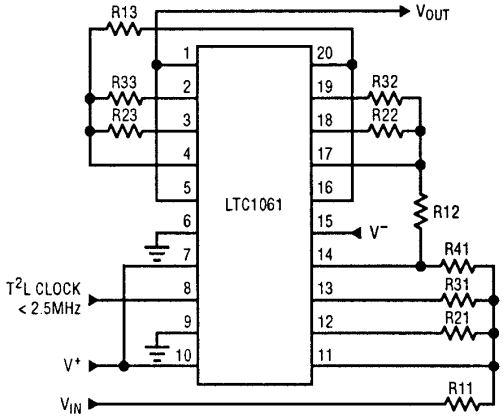


Figure 4. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

Since the input amplifier is within the resonant loop, its phase shift affects the high frequency operation of the filter and therefore, Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass, highpass and notch filters. Mode 3 as well as Mode 1 is a straightforward mode to use and the filter's dynamics can easily be optimized. Figure 5 illustrates a 6th order lowpass Butterworth filter operating with up to 40kHz cutoff frequency and with up to 200kHz input frequency. Sides A, B are connected in Mode 1 while side C is connected in Mode 3. The lower Q section was placed in side C, Mode 3, to eliminate any early Q enhancement. This could happen when the clock approaches 2MHz. The measured frequency response is shown in Figure 6. The attenuation floor is limited by the crosstalk between the three different sections operating with a clock frequency above 1MHz. The measured wideband noise was 150μV_{RMS}. For limited temperature range the filter of Figure 5 works up to 2.5MHz clock frequency thus yielding a 50kHz cutoff.



HARMONIC DISTORTION WITH f_{CLK} = 2MHz	
f_{IN}	2ND HARMONIC
10kHz, 1V_{RMS}	–74dB
20kHz, 1V_{RMS}	–62dB
30kHz, 1V_{RMS}	–62dB
40kHz, 1V_{RMS}	–62dB

STANDARD 1% RESISTOR VALUES	
R11 = 20k	R21 = 20k
R31 = 11k	R41 = 20k
R12 = 20k	R22 = 20k
R32 = 14k	R23 = 10k
R13 = 10k	R33 = 17.8k

LTC1061 F05

Figure 5. 6th Order Butterworth Lowpass Filter with Cutoff Frequency up to 45kHz

MODES OF OPERATION

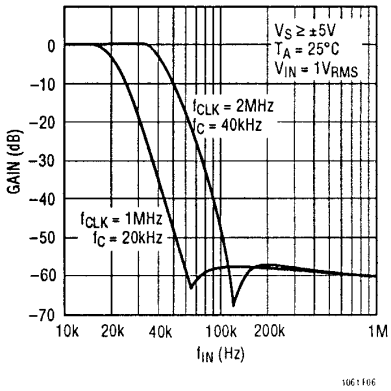
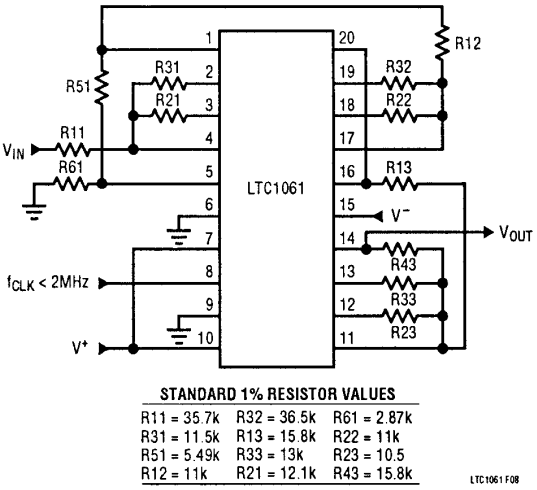


Figure 6. Measures Frequency Response of the Lowpass Butterworth Filter of Figure 3.

2. Secondary Modes: Mode 1b – It is derived from Mode 1. In Mode 1b, Figure 7, two additional resistors, R5 and R6, are added to attenuate the amount of voltage fed back from the lowpass output into the input of the S_A (S_B) switched capacitor summer. This allows the filter clock-to-center frequency ratio to be adjusted beyond 50:1 (or 100:1). Mode 1b still maintains the speed advantages of Mode 1. Figure 8 shows the 3 lowpass sections of the LTC1061 in cascade resulting in a Chebyshev lowpass filter. The side A of the IC is connected in Mode 1b to provide the first resonant frequency below the cutoff frequency of the filter. The practical ripple, obtained by using a non-A version of the LTC1061 and 1% standard resistor values, was 0.15dB. For this 6th order lowpass, the textbook Qs and center frequencies normalized to the ripple bandwidth are: Q1 = 0.55, f_{01} = 0.71, Q2 = 1.03, F_{02} = 0.969, Q3 = 3.4, F_{03} = 1.17. The design was done with speed in mind. The higher (Q3, F_{03}) section was in Mode 1 and placed in the side B of the LTC1061. The remaining two center frequencies were then normalized with respect to the center frequency of side B; this changes the ratio of clock-to-cutoff frequency from 50:1 to $50 \times 1.17 = 58.5:1$. As shown in Figure 9, the maximum cutoff frequency is about 33kHz. The total wideband output noise is 220μV_{RMS} and the measured output DC offset voltage is 60mV.



STANDARD 1% RESISTOR VALUES

R11 = 35.7k	R32 = 36.5k	R61 = 2.87k
R31 = 11.5k	R13 = 15.8k	R22 = 11k
R51 = 5.49k	R33 = 13k	R23 = 10.5
R12 = 11k	R21 = 12.1k	R43 = 15.8k

Figure 8. 6th Order Chebyshev, Lowpass Filter Using 3 Different Modes of Operation for Speed Optimization

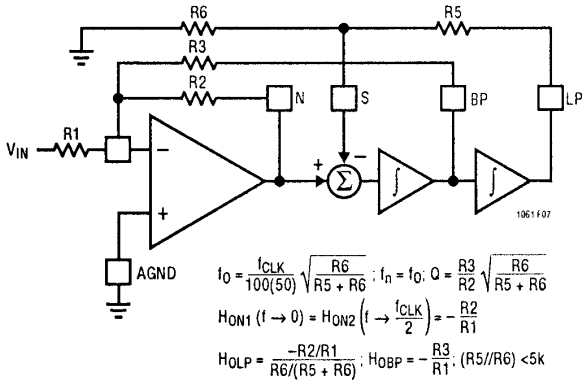


Figure 7. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

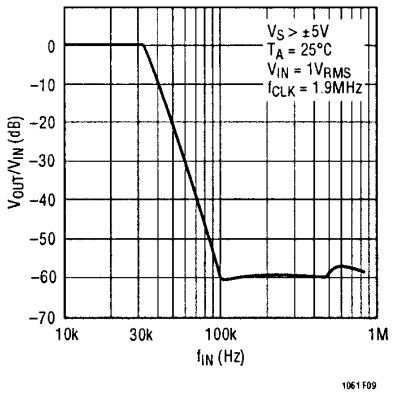


Figure 9. Amplitude Response of the 6th Order Chebyshev Lowpass Filter of Figure 8

MODES OF OPERATION

Another example of Mode 1b is illustrated on the front page of the data sheet. The cascading sequence of this 6th order bandpass filter is shown in block diagram form, Figure 10a. the filter is geometrically centered around the side B of the LTC1061 connected in Mode 1. This dictates a clock-to-center frequency ratio of 50:1 or 100:1. The side A of the IC operates in Mode 1b to provide the lower center frequency of 0.95 and still share the same clock with the rest of the filter. With this approach the bandpass filter can operate with center frequencies up to 24kHz. The speed of the filter could be further improved by using Mode 1 to lock the higher resonant frequency of 1.05 and higher Q or 31.9 to the clock, Figure 10b, thus changing the clock to center frequency ratio to 52.6:1.

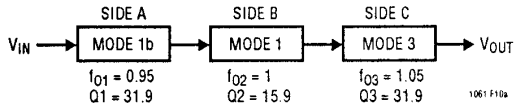


Figure 10a. Cascading Sequence of the Bandpass Filter Shown on the Front Page, with (f_{CLK}/f_O) = 50:1 or 100:1

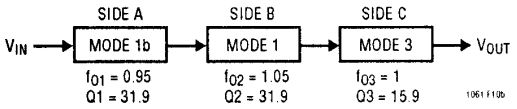
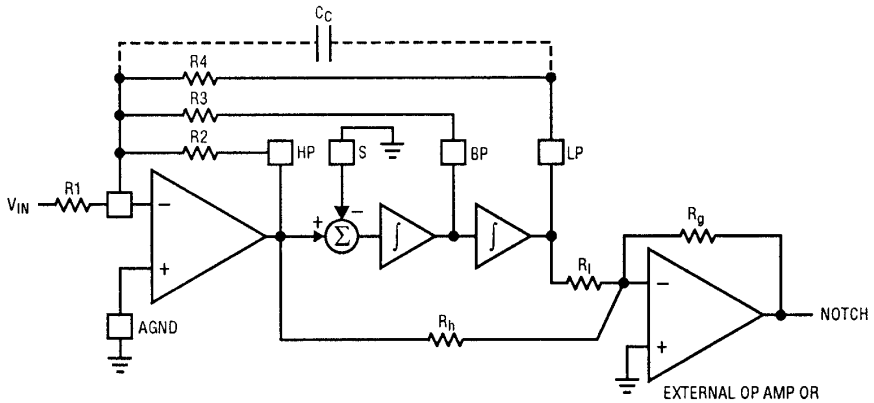


Figure 10b. Cascading Sequence of the Same Filter for Speed Optimization, and with (f_{CLK}/f_O) = 52.6:1

Mode 3a – This is an extension of Mode 3 where the highpass and lowpass outputs are summed through two external resistors R_h and R_l to create a notch, Figure 11. Mode 3a is very versatile because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 11 is not always required. When cascading the sections of the LTC1061, the highpass and lowpass outputs can be summed directly into the inverting input of the next section. Figure 12 shows an LTC1061 providing a 6th order elliptic bandpass or notch response. Sides C and B are connected in Mode 3a while side A is connected in Mode 1 and uses only two resistors. The resulting filter response is then geometrically symmetrical around either the center frequency of side A (for bandpass responses) or the notch frequency of side A (for notch responses).



$$f_O = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R_h}{R_l}};\ H_{OHP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{OLP} = -\frac{R4}{R1}$$

$$H_{ON1}(f \to 0) = \frac{R_g}{R_l} \times \frac{R4}{R1};\ H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times \frac{R2}{R1};\ H_{ON}(f = f_O) = Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)$$

$$Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}}$$

NOTE: FOR Q > 5 AND f_{CLK} > 1MHz, ADD C_C SUCH AS $C_C \cong \frac{0.16}{R4 \times 1.2MHz}$

Figure 11. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

MODES OF OPERATION

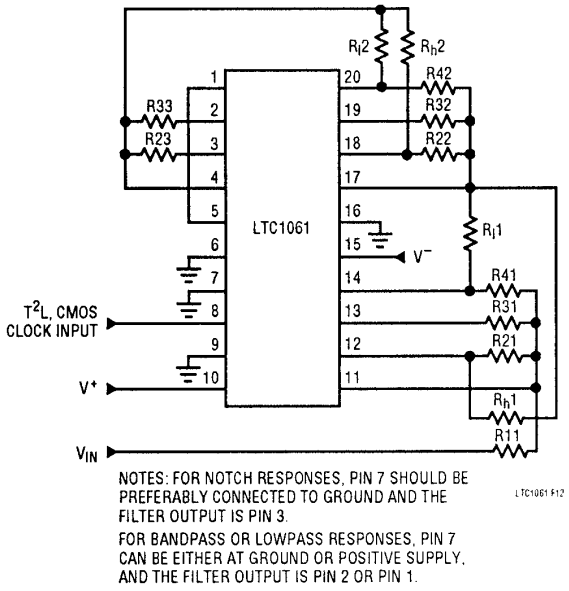


Figure 12. 6th Order Elliptic Bandpass, Lowpass or Notch Topology

Figure 13 shows the measured frequency response of the circuit Figure 12 configured to provide a notch function. The filter output is taken out of pin 3. The resistor values are standard 1%.

The ratio of the 0dB width, BW1, to the notch width BW2, is 5:1 and matches the theoretical design value. The measured notch depth was –53dB versus –56dB theoretical and the clock-to-center notch frequency ratio is 100:1.

Figure 14 shows the measured frequency response of the circuit topology, Figure 12, but with pole/zero locations configured to provide a high Q, 6th order elliptic bandpass filter operating with a clock-to-center frequency ratio of 50:1 or 100:1. The theoretical passband ripple, stopband attenuation and stopband to ripple bandwidth ratio are 0.5dB, 56dB, 5:1 respectively. The obtained results with 1% standard resistor values closely match the theoretical frequency response. For this application, the normalized center frequencies, Qs, and notch frequencies are (f_{O1} = 0.969, Q1 = 54.3, f_{n1} = 0.84, f_{O2} = 1.031, Q2 = 54.3, f_{n2} = 1.187, f_{O3} = 1, Q3 = 26.2). The output of the filter is the BP output of Side A, Pin 2.

Lowpass filters with stopband notches can also be realized by using Figure 12 provided that 6th order lowpass filter approximations with 2 stopband notches can be synthesized. Literature describing elliptic double terminated (RLC)

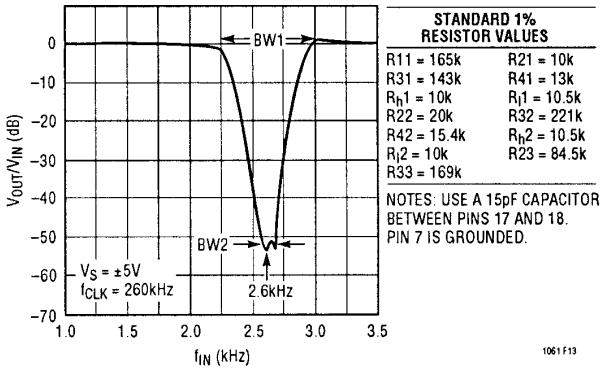


Figure 13. Resistor Values and Amplitude Response of Figure 12 Topology. The Notch is Centered at 2600Hz.

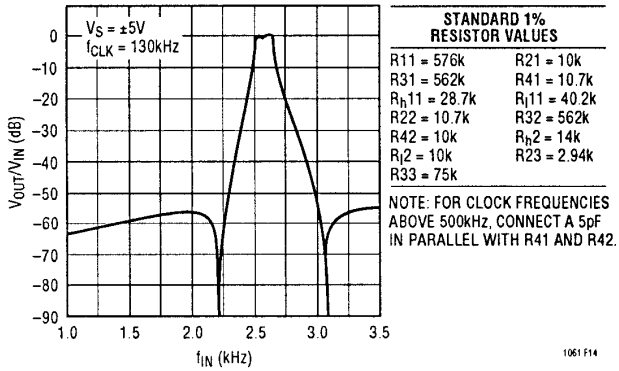


Figure 14. Resistor Values and Amplitude Response of Figure 12 Topology. The Bandpass Filter is Centered Around 2600Hz when Operating with a 130kHz Clock.

MODES OF OPERATION

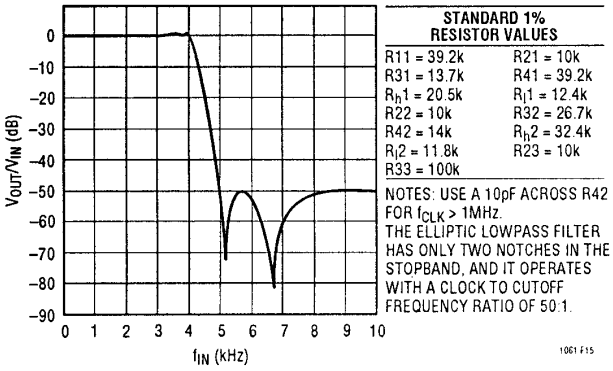


Figure 15. Resistor Values and Amplitude Response of the Topology of Figure 12.

passive ladder filters provide enough data to synthesize the above filters. The measured amplitude response of such a lowpass is shown in Figure 15 where the filter output is taken out of side A's Pin 1, Figure 12. The clock-to-center frequency ratio can be either 50:1 or 100:1 because the last stage of the LTC1061 operates in Mode 1 with a center frequency very close to the overall cutoff frequency of the lowpass filter.

In Figure 16, all three sides of the LTC1061 are connected in Mode 3a. This topology is useful for elliptic highpass and notch filters with clock-to-cutoff (or notch) frequency ratio higher than 100:1. This is often required to extend the allowed input signal frequency range and to avoid premature aliasing. Figure 16 is also a versatile, general purpose architecture providing 3 notches and 4 pole pairs, and there is no restriction on the location of the poles with respect to the notch frequencies. The drawbacks, when compared to Figure 12, are the use of an external op amp and the increased number of the required external resistors.

Figure 17 shows the measured frequency of a 6th order highpass elliptic filter operating with 250:1 clock-to-cutoff frequency ratio. With a 1MHz clock, for instance, the filter yields a 4kHz cutoff frequency, thus allowing an input frequency range beyond 100kHz. Band limiting can be easily added by placing a capacitor across the feedback resistor of the external op amp of Figure 16.

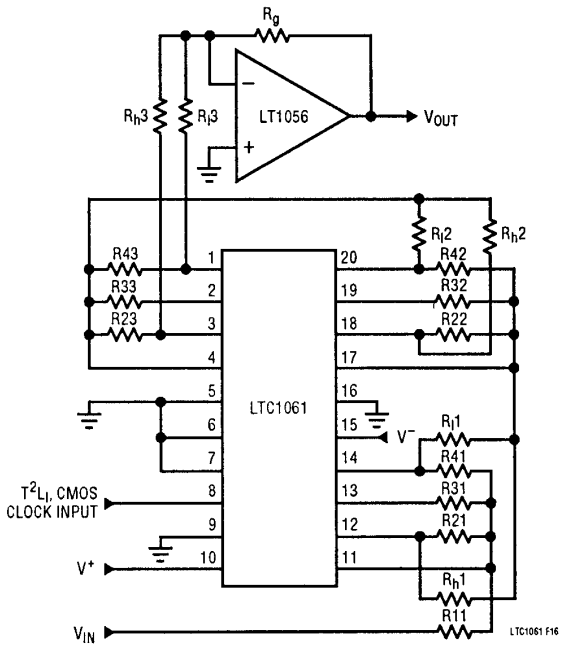


Figure 16. Using an External Op Amp to Connect all 3 Sides of the LTC1061 in Mode 3a.

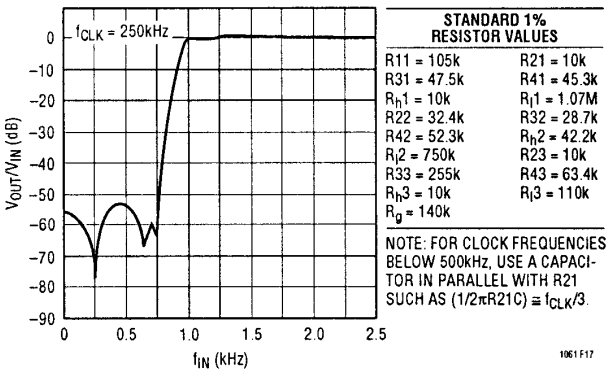


Figure 17. Measured Amplitude Response of the Topology of Figure 16, Configured to Provide a 6th Order Elliptic Highpass Filter Operating with a Clock-to-Cutoff Frequency Ratio of 250:1.

MODES OF OPERATION

Figure 18 shows the plotted amplitude responses of a 6th order notch filter operating again with a clock-to-center notch frequency ratio of 250:1. The theoretical notch depth is 70dB and when the notch is centered at 1kHz its width is 50Hz. Two small, noncritical capacitors were used across the R21 and R22 resistors of Figure 16, to band-limit the first two highpass outputs such that the practical notch depth will approach the theoretical value. With these two fixed capacitors, the notch frequency can be swept within a 3:1 range.

When the circuit of Figure 16 is used to realize lowpass elliptic filters, a capacitor across R_g raises the order of the filter and at the same time eliminates any small clock feedthrough. This is shown in Figure 19 where the amplitude response of the filter is plotted for 3 different cutoff frequencies. When the clock frequency equals or exceeds 1MHz, the stopband notches lose their depth due to the finite bandwidth of the internal op amps and to the small crosstalk between the different sides of the LTC1061. The lowpass filter, however, does not lose its passband accuracy and it maintains nearly all of its attenuation slope. The theoretical performance of the 7th order lowpass filter of Figure 19 is 0.2dB passband ripple, 1.5:1 stopband-to-cutoff frequency ratio, and 73dB stopband attenuation. Without any tuning, the obtained results closely approximate the textbook response.

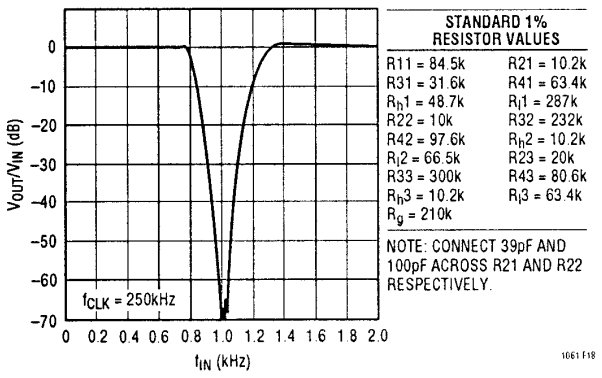


Figure 18. 6th Order Band Reject Filter Operating with a Clock-to-Center Notch Frequency Ratio of 250:1. The Ratio of 0dB to the –65dB Notch Width is 8:1.

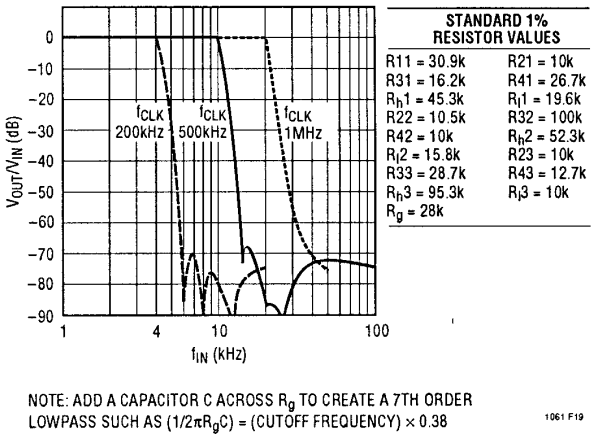


Figure 19. Frequency Responses of a 7th Order Lowpass Elliptic Filter Realized with Figure 16 Topology.

Mode 2 – This is a combination of Mode 1 and Mode 3, Figure 20. With Mode 2, the clock-to-center frequency ratio, f_{CLK}/f_O, is always less than 50:1 or 100:1. When compared to Mode 3 and for applications requiring 2nd order section with f_{CLK}/f_O slightly less than 100 or 50:1, Mode 2 provides less sensitivity to resistor tolerances. As in Mode 1, Mode 2 has a notch output which directly depends on the clock frequency and therefore the notch frequency is always less than the center frequency, f_O, of the 2nd order section.

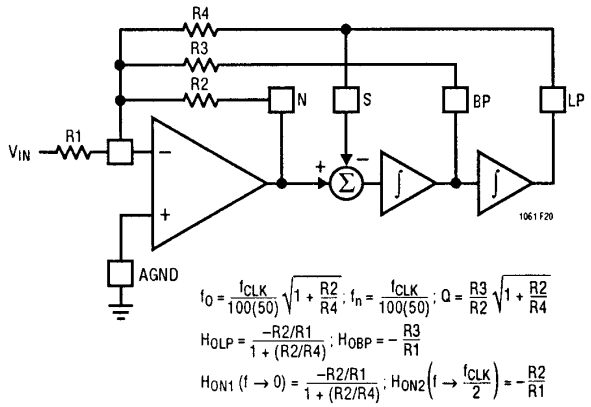


Figure 20. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass.

MODES OF OPERATION

Figure 21 shows the side A of the LTC1061 connected in Mode 2 while sides B and C are in Mode 3a. This topology can be used to synthesize elliptic bandpass, highpass and notch filters. The elliptic highpass of Figure 17 is synthesized again, Figure 22, but the clock is now locked onto the higher frequency notch provided by the side A of the LTC1061. As shown in Figure 22, the highpass corner frequency is 3.93kHz and the higher notch frequency is 3kHz while the filter operates with a 300kHz clock. The center frequencies, Qs, and notches of Figure 22, when normalized to the highpass cutoff frequency, are (f_{O1} = 1.17, Q1 = 2.24, f_{n1} = 0.242, f_{O2} = 1.96, Q2 = 0.7, f_{n2} = 0.6, f_{O3} = 0.987, f_{n3} = 0.753, Q3 = 10). When compared with the topology of Figure 16, this approach uses lower and more restricted clock frequencies. The obtained notch in Mode 2 is shallower although the topology is more efficient.

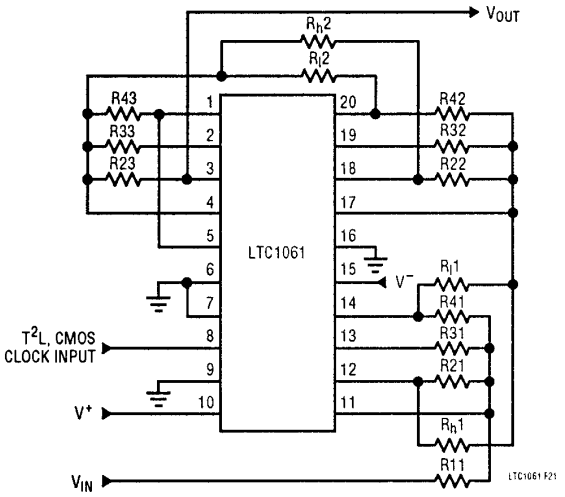


Figure 21. LTC1061 with Side A is Connected in Mode 2 While Side B, C are in Mode 3a. Topology is Useful for Elliptic Highpass, Notch and Bandpass Filters.

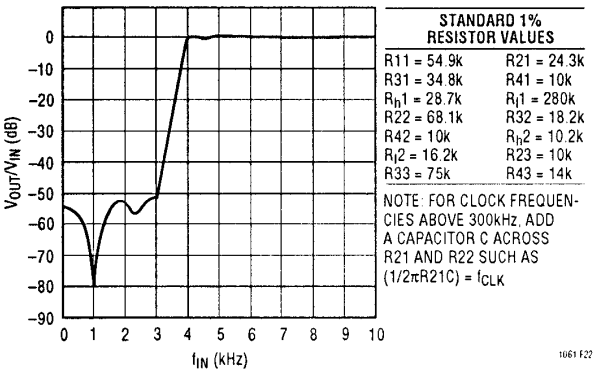


Figure 22. 6th Order Elliptic Highpass Filter Operating with a Clock-to-Cutoff Frequency Ratio of 75:1, and Using the Topology of Figure 21.

Output Noise

The wideband RMS noise of the LTC1061 outputs is nearly independent from the clock frequency. The LTC1061 noise when operating with ±2.5V supply is lower, as Table 3 indicates. The noise at the bandpass and lowpass outputs increases rough as the $\sqrt{Q}$. Also the noise increases when the clock-to-center frequency ratio is altered with external resistors to exceed the internally set 100:1 or 50:1 ratios. Under this condition, the noise increases square root-wise.

Output Offsets

The equivalent input offsets of the LTC1061 are shown in Figure 23. The DC offset at the filter bandpass output is always equal to V_{OS3}. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 4 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

1. The Qs decrease
2. The ratio (f_{CLK}/f_O) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

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MODES OF OPERATION

Table 3. Wideband RMS Noise

V_S (±V)	f_{CLK}/f_O	NOTCH/HP (μV_{RMS})	BP (μV_{RMS})	LP (μV_{RMS})	CONDITIONS
5.0	50:1	45	55	70	Mode 1, R1 = R2 = R3
5.0	100:1	65	65	85	Q = 1
2.5	50:1	30	30	45	
2.5	100:1	40	40	60	
5.0	50:1	18	150	150	Mode 1, Q = 10
5.0	100:1	20	200	200	R1 = R3 for BP Out
2.5	50:1	15	100	100	R1 = R2 for LP Out
2.5	100:1	17	140	140	
5.0	50:1	57	57	62	Mode 3, R1 = R2 = R3 = R4
5.0	100:1	72	72	80	Q = 1
2.5	50:1	40	40	42	
2.5	100:1	50	50	53	
5.0	50:1	135	120	140	Mode 3, R2 = R4, Q = 10
5.0	100:1	170	160	185	R3 = R1 for BP Out
2.5	50:1	100	88	100	R4 = R1 for LP and HP Out
2.5	100:1	125	115	130	

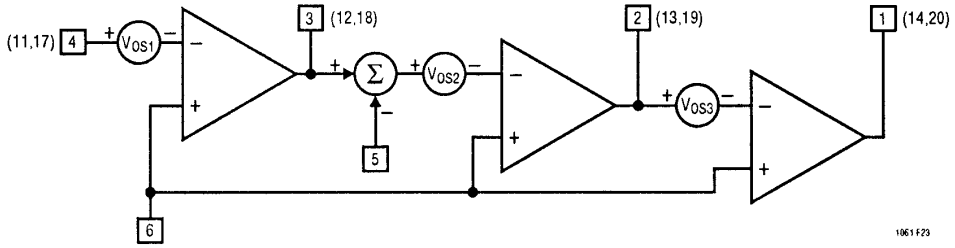


Figure 23. Equivalent Input Offsets of 1/3 LTC1061 Filter Building Block.

Table 4

MODE	V_{OSN} PIN 3 (18)	V_{OSBP} PIN 2 (19)	V_{OSLP} PIN 1 (20)
1	V_{OS1} [(1/Q) + 1 + ‖ H_{OLP} ‖] – V_{OS3}/Q	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	V_{OS1} [(1/Q) + 1 + R2/R1] – V_{OS3}/Q	V_{OS3}	~($V_{OSN} - V_{OS2}$)(1 + R5/R6)
2	[V_{OS1} (1 + R2/R1 + R2/R3 + R2/R4) – V_{OS3}(R2/R3)] × × [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	V_{OS1} (1 + R4/R1 + R4/R2 + R4/R3) – V_{OS2}(R4/R2) – V_{OS3} (R4/R3)

ANALOG DEVICES

Integrated Circuit True RMS-to-DC Converter

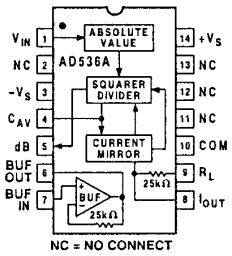
AD536A

FEATURES

True RMS-to-DC Conversion
Laser-Trimmed to High Accuracy
0.2% Max Error (AD536AK)
0.5% Max Error (AD536AJ)
Wide Response Capability:
Computes RMS of AC and DC Signals
450 kHz Bandwidth: V rms > 100 mV
2 MHz Bandwidth: V rms > 1 V
Signal Crest Factor of 7 for 1% Error
dB Output with 60 dB Range
Low Power: 1.2 mA Quiescent Current
Single or Dual Supply Operation
Monolithic Integrated Circuit
–55°C to +125°C Operation (AD536AS)

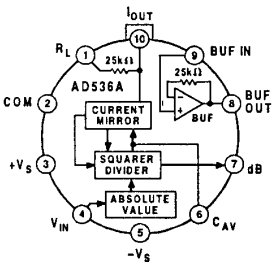
PIN CONFIGURATIONS AND FUNCTIONAL BLOCK DIAGRAMS

TO-116 (D-14) and Q-14 Package

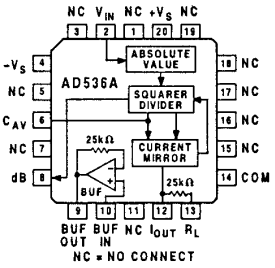


NC = NO CONNECT

TO-100 (H-10A) Package



LCC (E-20A) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300 kHz with 3 dB error for signal levels above 100 mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60 dB. Using an externally supplied reference current, the 0 dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full-scale accuracy at 7 V rms. As a result, no external trims are required to achieve the rated unit accuracy.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0°C to +70°C) applications, and one grade (S) rated for the –55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2 mV ±0.2% of reading, and the AD536AJ and AD536AS have maximum errors of ±5 mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-lead DIP or 10-pin TO-100 metal can. The AD536AS is also available in a 20-leadless hermetically sealed ceramic chip carrier.

REV. B

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536 and provides improved bandwidth and temperature drift specifications.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD536A–SPECIFICATIONS (@ +25°C, and ±15 V dc unless otherwise noted)

Model	AD536AJ Min	AD536AJ Typ	AD536AJ Max	AD536AK Min	AD536AK Typ	AD536AK Max	AD536AS Min	AD536AS Typ	AD536AS Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Figure 1)			±5 **±0.5**			**±2 ±0.2**			±5 **±0.5**	mV ± % of Reading
vs. Temperature, T_{MIN} to +70°C			±0.1 ±0.01			±0.05 ±0.005			**±0.1 ±0.005**	mV ± % of Reading/°C
+70°C to +125°C									**±0.3 ±0.005**	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error		±0.2			±0.1			±0.2		± % of Reading
Total Error, External Trim[1] (Figure 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR VS. CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		-0.1			-0.1			-0.1		% of Reading
Crest Factor = 7		-1.0			-1.0			-1.0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% Additional Error (0.09 dB)										
V_{IN} = 10 mV		5			5			5		kHz
V_{IN} = 100 mV		45			45			45		kHz
V_{IN} = 1 V		120			120			120		kHz
±3 dB Bandwidth										
V_{IN} = 10 mV		90			90			90		kHz
V_{IN} = 100 mV		450			450			450		kHz
V_{IN} = 1 V		2.3			2.3			2.3		MHz
AVERAGING TIME CONSTANT (Figure 5)		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ±15 V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, ±5 V Supplies		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, ±5 V Supplies			±7			±7			±7	V peak
Maximum Continuous Nondestructive Input Level (All Supply Voltages)			±25			±25			±25	V peak
Input Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
Input Offset Voltage		0.8	±2		0.5	±1		0.8	±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V_{IN} = COM (Figure 1)		±1	±2		±0.5	±1			±2	mV
vs. Temperature		±0.1			±0.1				**±0.2**	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ±15 V Supplies	0 to +11	+12.5		0 to +11	+12.5		0 to +11	+12.5		V
±5 V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT (Figure 13)										
Error, V_{IN} 7 mV to 7 V rms, 0 dB = 1 V rms		±0.4	**±0.6**		±0.2	**±0.3**		±0.5	**±0.6**	dB
Scale Factor		-3			-3			-3		mV/dB
Scale Factor TC (Uncompensated, see Figure 1 for Temperature Compensation)		-0.033			-0.033			-0.033		dB/°C
		+0.33			+0.33			+0.33		% of Reading/°C
I_{REF} for 0 dB = 1 V rms	5	20	**80**	5	20	**80**	5	20	**80**	μA
I_{REF} Range	1		100	1		100	1		100	μA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		μA/V rms
I_{OUT} Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
Output Resistance	20	25	30	20	25	30	20	25	30	kΩ
Voltage Compliance		$-V_S$ to $(+V_S$ -2.5 V)			$-V_S$ to $(+V_S$ -2.5 V)			$-V_S$ to $(+V_S$ -2.5 V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$ to $(+V_S$ -2.5 V)			$-V_S$ to $(+V_S$ -2.5 V)			$-V_S$ to $(+V_S$ -2.5 V)			V
Input Offset Voltage, R_S = 25 k		±0.5	±4		±0.5	±4		±0.5	±4	mV
Input Bias Current		20	**60**		20	**60**		20	**60**	nA
Input Resistance		10^6			10^6			10^6		Ω
Output Current	(+5 mA, -130 μA)			(+5 mA, -130 μA)			(+5 mA, -130 μA)			
Short Circuit Current		20			20			20		mA
Output Resistance			0.5			0.5			0.5	Ω
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/μs
POWER SUPPLY										
Voltage Rated Performance		±15			±15			±15		V
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S, 5 V to 36 V, T_{MIN} to T_{MAX}		1.2	2		1.2	2		1.2	2	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	-55		+125	°C
Storage	-55		+150	-55		+150	-55		+150	°C
NUMBER OF TRANSISTORS		65			65			65		

NOTES

[1]Accuracy is specified for 0 V to 7 V rms, dc or 1 kHz sine wave input with the AD536A connected as in the figure referenced.

[2]Error vs. crest factor is specified as an additional error for 1 V rms rectangular pulse input, pulsewidth = 200 μs.

[3]Input voltages are expressed in volts rms, and error is percent of reading.

[4]With 2k external pull-down resistor.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
- Dual Supply ..... ±18 V
- Single Supply ..... +36 V

Internal Power Dissipation[2] ..... 500 mW
Maximum Input Voltage ..... ±25 V Peak
Buffer Maximum Input Voltage ..... $\pm V_S$
Maximum Input Voltage ..... ±25 V Peak
Storage Temperature Range ..... -55°C to +150°C
Operating Temperature Range
- AD536AJ/K ..... 0°C to +70°C
- AD536AS ..... -55°C to +125°C

Lead Temperature Range
- (Soldering 60 sec) ..... +300°C

ESD Rating ..... 1000 V

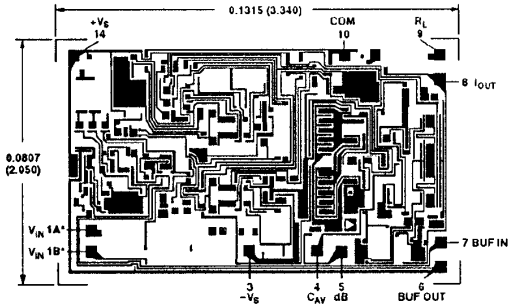
NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]10-Pin Header: θ_{JA} = 150°C/W; 20-Leadless LCC: θ_{JA} = 95°C/W; 14-Lead Size Brazed Ceramic DIP: θ_{JA} = 95°C/W.

CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-166 14-LEAD CERAMIC DIP PACKAGE.
NOTE
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.
THE AD536A IS AVAILABLE IN LASER TRIMMED CHIP FORM.
SUBSTRATE CONNECTED TO $-V_S$.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD536AJD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AKD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AJH	0°C to +70°C	Header	H-10A
AD536AKH	0°C to +70°C	Header	H-10A
AD536AJQ	0°C to +70°C	Cerdip	Q-14
AD536AKQ	0°C to +70°C	Cerdip	Q-14
AD536ASD	-55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASD/883B	-55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASE/883B	-55°C to +125°C	LCC	E-20A
AD536ASH	-55°C to +125°C	Header	H-10A
AD536ASH/883B	-55°C to +125°C	Header	H-10A
AD536AJCHIPS	0°C to +70°C	Die	
AD536AKH/+	0°C to +70°C	Header	H-10A
AD536ASCHIPS	-55°C to +125°C	Die	
5962-89805012A	-55°C to +125°C	LCC	E-20A
5962-8980501CA	-55°C to +125°C	Side Brazed Ceramic DIP	D-14
5962-8980501IA	-55°C to +125°C	Header	H-10A

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4 µF capacitor is used, the additional average error at 10 Hz will be 0.1%, at 3 Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with the input, as shown in Figure 3, the capacitor must be nonpolar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1 µF ceramic discs as near the device as possible.

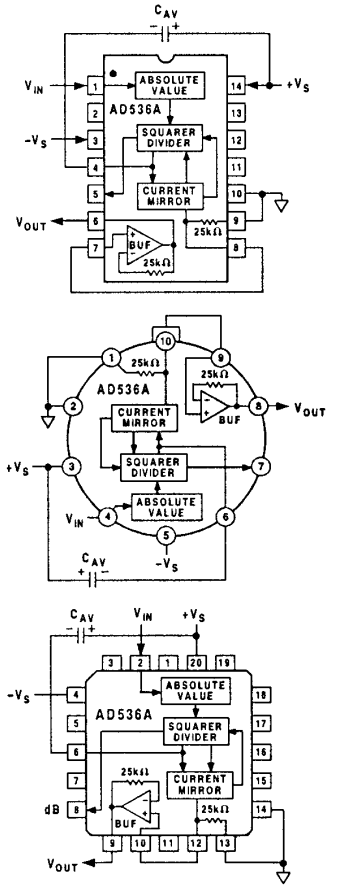


Figure 1. Standard RMS Connection

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 14. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25 kΩ resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25 kΩ resistor from ground. The output current is available at Pin 8 (Pin 10 on the "H" package) with a nominal scale of 40 μA per volt rms input positive out.

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R4 is used to trim the offset. Note that the offset trim circuit adds 365 Ω in series with the internal 25 kΩ resistor. This will cause a 1.5% increase in scale factor, which is trimmed out by using R1 as shown. Range of scale factor adjustment is ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R4 to give zero volts output from Pin 6. Alternatively, R4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1 kHz is the optimum frequency); then trim R1, to give the correct output from Pin 6, i.e., 1000 V dc input should give 1.000 V dc output. Of course, a ±1.000 V peak-to-peak sine wave should give a 0.707 V dc output. The remaining errors, as given in the specifications are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7 V rms full-scale range.

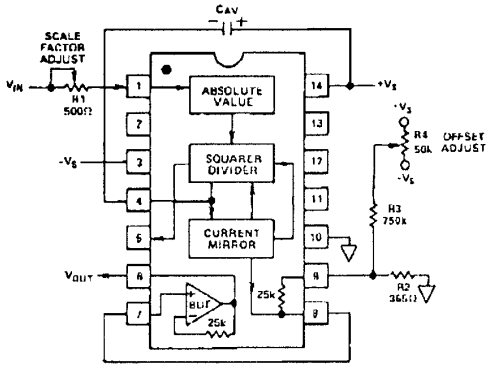


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at Pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 mA of current flows into Pin 10 (Pin 2 on the "H" package). AC input coupling requires only capacitor C2 as shown; a dc return is not necessary as it is provided internally. C2 is selected for the proper low frequency break point with the input resistance of 16.7 kΩ; for a cutoff at 10 Hz, C2 should be 1 μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 14. The load resistor, R_L, is necessary to provide output sink current.

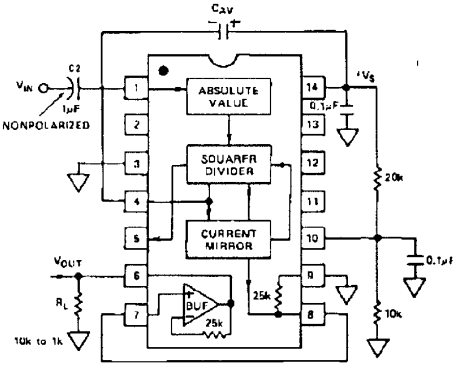


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly-varying dc signal, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

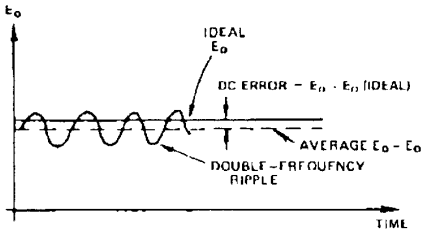


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given percent dc error above a given frequency using the standard rms connection.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will affect a tenfold reduction in ripple. When measuring waveforms with high crest

factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100 Hz pulse rate requires a 100 ms time constant, which corresponds to a 4 μF capacitor (time constant = 25 ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

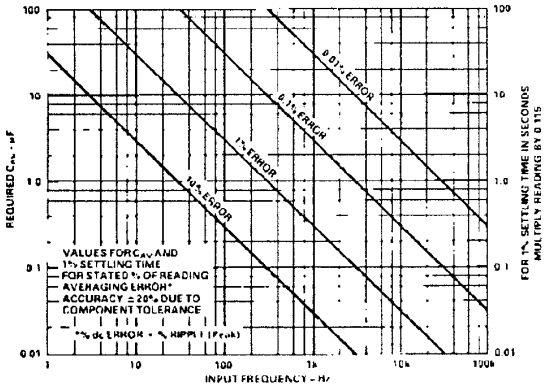


Figure 5. Error/Settling Time Graph for Use with the Standard rms Connection in Figure 1

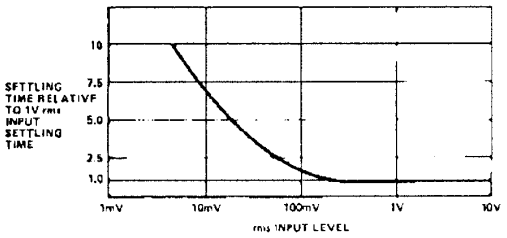


Figure 6. Settling Time vs. Input Level

A better method for reducing output ripple is the use of a "post-filter." Figure 7 shows a suggested circuit. If a single-pole filter is used (C3 removed, R_X shorted), and C2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8 and settling time is increased. For example, with C_{AV} = 1 μF and C2 = 2.2 μF, the ripple for a 60 Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C2, can, therefore, be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C2, and C3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explanation of these topics refer to the *RMS to DC Conversion Application Guide 2nd Edition*, available from Analog Devices.

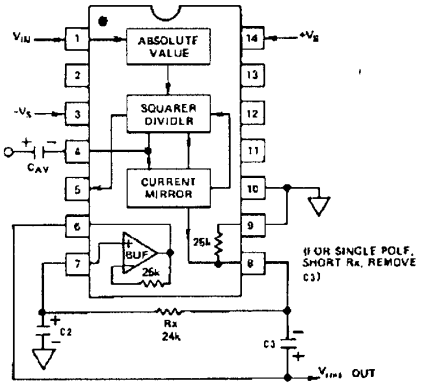


Figure 7. 2-Pole "Post" Filter

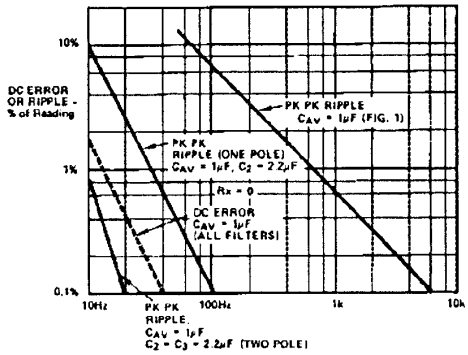


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straightforward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V\,rms = Avg.\left[\frac{V_{IN}^{\,2}}{V\,rms}\right]$$

AD536A

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2/I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low-pass filter formed by R1 and the externally connected capacitor, C_{AV}. If the R1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. [I_4], back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = Avg.\left[I_1^2/I_4\right] = I_1\ rms$$

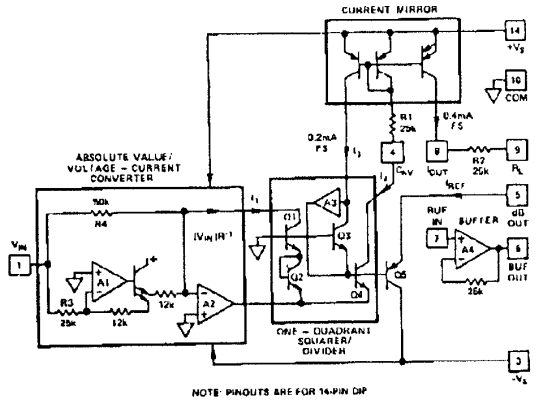


Figure 9. Simplified Schematic

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R2 and buffered by A4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R2\ I\ rms = V_{IN}\ rms$$

The dB output is derived from the emitter of Q3, since the voltage at this point is proportional to –log V_{IN}. Emitter follower, Q5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q5 approximates I_3.

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A is the logarithmic or decibel output. The internal circuit computing dB works accurately over a 60 dB range. The connections for dB measurements are shown in Figure 10. The user selects the 0 dB level by adjusting R1, for the proper 0 dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0 dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C scale factor drift of the dB output pin. The special T.C. resistor, R2, is available from Tel Labs in Londonderry, N.H. (model Q-81) or from Precision Resistor Inc., Hillside, N.J. (model PT146). The averaged temperature coefficients of resistors R2 and R3 develop the +3300 ppm needed to reverse compensate the dB output. The linear rms output is available at Pin 8 on DIP or Pin 10 on header device with an output impedance of 25 kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00 V dc or 1.00 V rms
2. Adjust R1 for dB out = 0.00 V
3. Set V_{IN} = +0.1 V dc or 0.10 V rms
4. Adjust R5 for dB out = –2.00 V

Any other desired 0 dB reference level can be used by setting V_{IN} and adjusting R1, accordingly. Note that adjusting R5 for the proper gain automatically gives the correct temperature compensation.

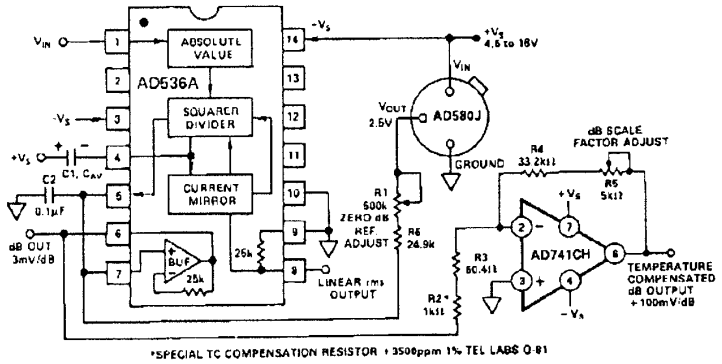


Figure 10. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 7 volts rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3 dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 120 kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100 µV) up to only 5 kHz.

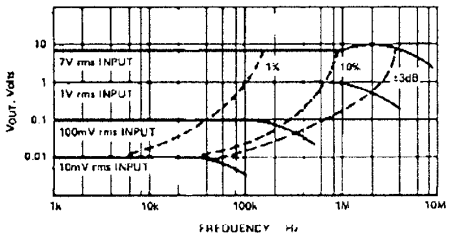


Figure 11. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (CF = V_P/V rms). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 ($CF = 1\sqrt{\eta}$).

Figure 12 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulsewidth 100 µs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 11 while maintaining a constant 1 volt rms input amplitude.

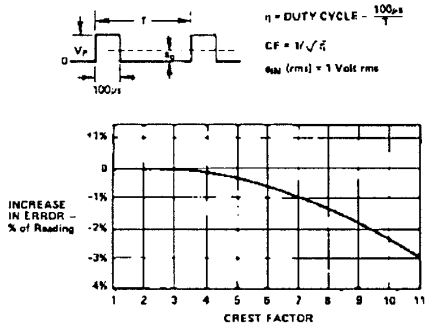


Figure 12. Error vs. Crest Factor

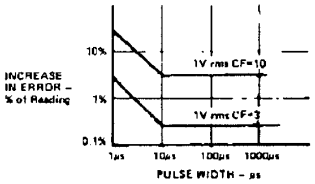


Figure 13. AD536A Error vs. Pulsewidth Rectangular Pulse

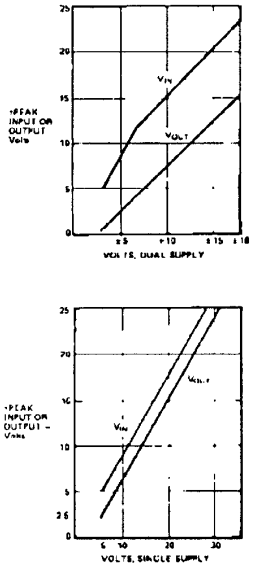


Figure 14. AD536A Input and Output Voltage Ranges vs. Supply

ANALOG DEVICES

Real-Time Analog Computational Unit (ACU)

AD538

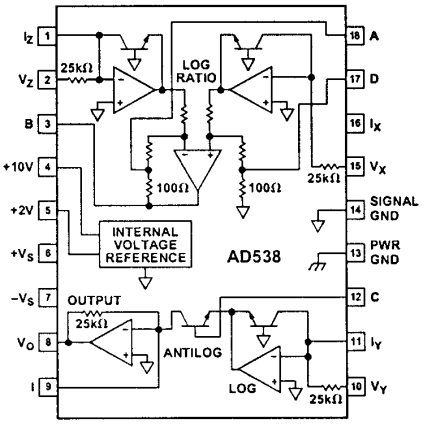
FEATURES

$V_{OUT} = V_Y \left(\frac{V_Z}{V_X}\right)^m$ Transfer Function
Wide Dynamic Range (Denominator) –1000:1
Simultaneous Multiplication and Division
Resistor-Programmable Powers and Roots
No External Trims Required
Low Input Offsets <100 μV
Low Error ±0.25% of Reading (100:1 Range)
+2 V and +10 V On-Chip References
Monolithic Construction

APPLICATIONS

One- or Two-Quadrant Mult/Div
Log Ratio Computation
Squaring/Square Rooting
Trigonometric Function Approximations
Linearization Via Curve Fitting
Precision AGC
Power Functions

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD538 is a monolithic real-time computational circuit that provides precision analog multiplication, division and exponentiation. The combination of low input and output offset voltages and excellent linearity results in accurate computation over an unusually wide input dynamic range. Laser wafer trimming makes multiplication and division with errors as low as 0.25% of reading possible, while typical output offsets of 100 μV or less add to the overall off-the-shelf performance level. Real-time analog signal processing is further enhanced by the device's 400 kHz bandwidth.

The AD538's overall transfer function is $V_O = V_Y (V_Z/V_X)^m$. Programming a particular function is via pin strapping. No external components are required for one-quadrant (positive input) multiplication and division. Two-quadrant (bipolar numerator) division is possible with the use of external level shifting and scaling resistors. The desired scale factor for both multiplication and division can be set using the on-chip +2 V or +10 V references, or controlled externally to provide simultaneous multiplication and division. Exponentiation with an m value from 0.2 to 5 can be implemented with the addition of one or two external resistors.

Direct log ratio computation is possible by using only the log ratio and output sections of the chip. Access to the multiple summing junctions adds further to the AD538's flexibility. Finally, a wide power supply range of ±4.5 V to ±18 V allows operation from standard ±5 V, ±12 V and ±15 V supplies.

The AD538 is available in two accuracy grades (A and B) over the industrial (–25°C to +85°C) temperature range and one grade (S) over the military (–55°C to +125°C) temperature range. The device is packaged in an 18-lead TO-118 hermetic side-brazed ceramic DIP. A-grade chips are also available.

PRODUCT HIGHLIGHTS

1. Real-time analog multiplication, division and exponentiation.
2. High accuracy analog division with a wide input dynamic range.
3. On-chip +2 V or +10 V scaling reference voltages.
4. Both voltage and current (summing) input modes.
5. Monolithic construction with lower cost and higher reliability than hybrid and modular circuits.

RE-EXAMINATION OF MULTIPLIER/DIVIDER ACCURACY

Traditionally, the "accuracy" (actually the errors) of analog multipliers and dividers have been specified in terms of percent of full scale. Thus specified, a 1% multiplier error with a 10 V full-scale output would mean a worst case error of +100 mV at "any" level within its designated output range. While this type of error specification is easy to test evaluate, and interpret, it can leave the user guessing as to how useful the multiplier actually is at low output levels, those approaching the specified error limit (in this case) 100 mV.

The AD538's error sources do not follow the percent of full-scale approach to specification, thus it more optimally fits the needs of the very wide dynamic range applications for which it is best suited. Rather than as a percent of full scale, the AD538's error as a multiplier or divider for a 100:1 (100 mV to 10 V) input range is specified as the sum of two error components: a percent of reading (ideal output) term plus a fixed output offset. Following this format the AD538AD, operating as a multiplier or divider with inputs down to 100 mV, has a maximum error of ±1% of reading ±500 µV. Some sample total error calculations for both grades over the 100:1 input range are illustrated in the chart below. This error specification format is a familiar one to designers and users of digital voltmeters where error is specified as a percent of reading ± a certain number of digits on the meter readout.

For operation as a multiplier or divider over a wider dynamic range (>100:1), the AD538 has a more detailed error specification that is the sum of three components: a percent of reading term, an output offset term and an input offset term for the V_Y/V_X log ratio section. A sample application of this specification, taken from Table I, for the AD538AD with V_Y = 1 V, V_Z = 100 mV and V_X = 10 mV would yield a maximum error of ±2.0% of reading ±500 µV ±(1 V + 100 mV)/10 mV × 250 µV or ±2.0% of reading ±500 µV ± 27.5 mV. This example illustrates that with very low level inputs the AD538's incremental gain $(V_Y + V_Z)/V_X$ has increased to make the input offset contribution to error substantial.

Table I. Sample Error Calculation Chart (Worst Case)

	V_Y Input (in V)	V_Z Input (in V)	V_X Input (in V)	Ideal Output (in V)	Total Offset Error Term (in mV)	% of Reading Error Term (in mV)	Total Error Summation (in mV)	Total Error Summation as a % of the Ideal Output
100:1 INPUT RANGE	10	10	10	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
Total Error = ±% rdg ±Output V_{OS}	10	0.1	0.1	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	1	1	1	1	0.5 (AD) 0.25 (BD)	10 (AD) 5 (BD)	10.5 (AD) 5.25 (BD)	1.05 (AD) 0.5 (BD)
	0.1	0.1	0.1	0.1	0.5 (AD) 0.25 (BD)	1 (AD) 0.5 (BD)	1.5 (AD) 0.75 (BD)	1.5 (AD) 0.75 (BD)
WIDE DYNAMIC RANGE	1	0.10	0.01	10	28 (AD) 16.75 (BD)	200 (AD) 100 (BD)	228 (AD) 116.75 (BD)	2.28 (AD) 1.17 (BD)
Total Error = ±% rdg ±Output V_{OS} ±Input V_{OS} × $(V_Y + V_Z)/V_X$	10	0.05	2	0.25	1.76 (AD) 1 (BD)	5 (AD) 2.5 (BD)	6.76 (AD) 3.5 (BD)	2.7 (AD) 1.4 (BD)
	5	0.01	0.01	5	125.75 (AD) 75.4 (BD)	100 (AD) 50 (BD)	225.75 (AD) 125.4 (BD)	4.52 (AD) 2.51 (BD)
	10	0.01	0.1	1	25.53 (AD) 15.27 (BD)	20 (AD) 10 (BD)	45.53 (AD) 25.27 (BD)	4.55 (AD) 2.53 (BD)

AD538–SPECIFICATIONS ($V_S = \pm 15$ V, $T_A = +25°C$ unless otherwise noted)

Parameters	Conditions	AD538AD Min	AD538AD Typ	AD538AD Max	AD538BD Min	AD538BD Typ	AD538BD Max	AD538SD Min	AD538SD Typ	AD538SD Max	Units
MULTIPLIER DIVIDER PERFORMANCE											
Nominal Transfer Function											
	10 V ≥ V_X, V_Y, V_Z ≥ 0		$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$		
	400 µA ≥ I_X, I_Y, I_Z ≥ 0		$V_O = 25\ k\Omega \times I_Y \left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25\ k\Omega \times I_Y \left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25\ k\Omega \times I_Y \left(\frac{I_Z}{I_X}\right)^m$		
Total Error Terms	100 mV ≤ V_X ≤ 10 V		±0.5	±1		±0.25	±0.5		±0.5	±1	% of Reading +
100:1 Input Range[1]	100 mV ≤ V_Y ≤ 10 V		±200	±500		±100	±250		±200	±500	µV
	100 mV ≤ V_Z ≤ 10 V, V_Z ≤ 10 V_X, m = 1.0										
	$T_A = T_{MIN}$ to T_{MAX}		±1	±2		±0.5	±1		±1.25	±2.5	% of Reading +
			±450	±750		±350	±500		±750	±1000	µV
Wide Dynamic Range[2]	10 mV ≤ V_X ≤ 10 V		±1	±2		±0.5	±1		±1	±2	% of Reading +
	1 mV ≤ V_Y ≤ 10 V		±200	±500		±100	±250		±200	±500	µV +
	0 mV ≤ V_Z ≤ 10 V, V_Z ≤ 10 V_X, m = 1.0		±100	±250		±750	±150		±200	±250	µV × $(V_Y + V_Z)/V_X$
	$T_A = T_{MIN}$ to T_{MAX}		±1	±3		±1	±2		±2	±4	% of Reading +
			±450	±750		±350	±500		±750	±1000	µV +
			±450	±750		±350	±500		±750	±1000	µV × $(V_Y + V_Z)/V_X$
Exponent (m) Range	$T_A = T_{MIN}$ to T_{MAX}	0.2		5	0.2		5	0.2		5	
OUTPUT CHARACTERISTICS											
Offset Voltage	V_Y = 0, V_C = -600 mV		±200	±500		±100	±250		±200	±500	µV
	$T_A = T_{MIN}$ to T_{MAX}		±450	±750		±350	±500		±750	±1000	µV
Output Voltage Swing	R_L = 2 kΩ	-11		+11	-11		+11	-11		+11	V
Output Current		5	10		5	10		5	10		mA
FREQUENCY RESPONSE											
Slew Rate			1.4			1.4			1.4		V/µs
Small Signal Bandwidth	100 mV ≤ V_Y, V_Z, V_X ≤ 10 V		400			400			400		kHz
VOLTAGE REFERENCE											
Accuracy	V_{REF} = 10 V or 2 V		±25	±50		±15	±25		±25	±50	mV
Additional Error	$T_A = T_{MIN}$ or T_{MAX}		±20	±30		±20	±30		±30	±50	mV
Output Current	V_{REF} = 10 V to 2 V	1	2.5		1	2.5		1	2.5		mA
Power Supply Rejection											
+2 V = V_{REF}	±4.5 V ≤ V_S ≤ ±18 V		300	600		300	600		300	600	µV/V
+10 V = V_{REF}	±13 V ≤ V_S ≤ ±18 V		200	500		200	500		200	500	µV/V
POWER SUPPLY											
Rated	R_L = 2 kΩ		±15			±15			±15		V
Operating Range[3]		±4.5		±18	±4.5		±18	±4.5		±18	V
PSRR	±4.5 V < V_S < ±18 V, V_X = V_Y = V_Z = 1 V, V_{OUT} = 1 V		0.5	0.1		0.05	0.1		0.5	0.1	%/V
Quiescent Current			4.5	7		4.5	7		4.5	7	mA
TEMPERATURE RANGE											
Rated		-25		+85	-25		+85	-55		+125	°C
Storage		-65		+150	-65		+150	-65		+150	°C
PACKAGE OPTIONS											
Ceramic (D-18)			AD538AD			AD538BD			AD538SD AD538SD/883B		
Chips			AD538ACHIPS								

NOTES

[1]Over the 100 mV to 10 V operating range total error is the sum of a percent of reading term and an output offset. With this input dynamic range the input offset contribution to total error is negligible compared to the percent of reading error. Thus, it is specified indirectly as a part of the percent of reading error.

[2]The most accurate representation of total error with low level inputs is the summation of a percent of reading term, an output offset and an input offset multiplied by the incremental gain $(V_Y + V_Z)/V_X$.

[3]When using supplies below ±13 V, the 10 V reference pin *must* be connected to the 2 V pin in order for the AD538 to operate correctly.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

AD538

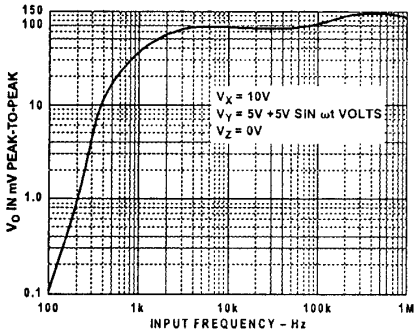


Figure 7. V_Y Feedthrough vs. Frequency

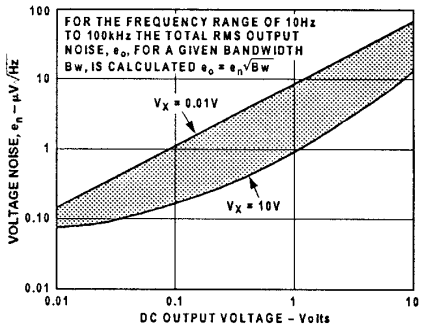


Figure 8. 1 kHz Output Noise Spectral Density vs. DC Output Voltage

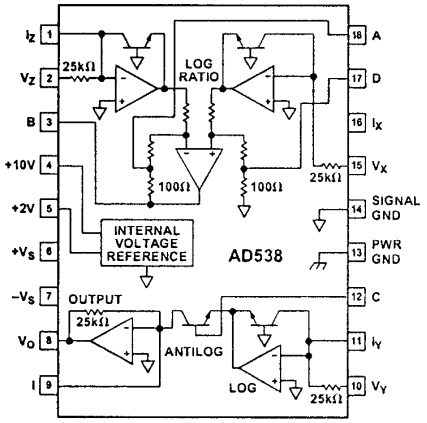


Figure 9. Functional Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figures 9 and 10, the V_Z and V_X inputs connect directly to the AD538's input log ratio amplifiers. This subsection provides an output voltage proportional to the natural log of input voltage V_Z, minus the natural log of input voltage V_X. The output of the log ratio subsection at B can be expressed by the transfer function:

$$V_B = \frac{kT}{q} \ln\left(\frac{V_Z}{V_X}\right)$$

where $k = 1.3806 \times 10^{-23}$ J/K,
$q = 1.60219 \times 10^{-19}$ C,
T is in Kelvins.

The log ratio configuration may be used alone, if correctly temperature compensated and scaled to the desired output level (see Applications section).

Under normal operation, the log-ratio output will be directly connected to a second functional block at input C, the antilog subsection. This section performs the antilog according to the transfer function:

$$V_O = V_Y e^{V_C \frac{q}{kT}}$$

As with the log-ratio circuit included in the AD538, the user may use the antilog subsection by itself. When both subsections are combined, the output at B is tied to C, the transfer function of the AD538 computational unit is:

$$V_O = V_Y e^{\frac{kT}{q} \ln\left(\frac{V_Z}{V_X}\right)}; V_B = V_C$$

which reduces to:

$$V_O = V_Y \left(\frac{V_Z}{V_X}\right)$$

Finally, by increasing the gain, or attenuating the output of the log ratio subsection via resistor programming, it is possible to raise the quantity V_Z/V_X to the m^{th} power. Without external programming, m is unity. Thus the overall AD538 transfer function equals:

$$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$$

where $0.2 < m < 5$.

When the AD538 is used as an analog divider, the V_Y input can be used to multiply the ratio V_Z/V_X by a convenient scale factor. The actual multiplication by the V_Y input signal is accomplished by adding the log of the V_Y input signal to the signal at C, which is already in the log domain.

STABILITY PRECAUTIONS

At higher frequencies, the multistaged signal path of the AD538, as illustrated in Figure 10, can result in large phase shifts. If a condition of high incremental gain exists along that path (e.g., $V_O = V_Y \times V_Z/V_X = 10\ V \times 10\ mV/10\ mV = 10\ V$ so that $\Delta V_O/\Delta V_X = 1000$), then small amounts of capacitive feedback from V_O to the current inputs I_Z or I_X can result in instability. Appropriate care should be exercised in board layout to prevent capacitive feedback mechanisms under these conditions.

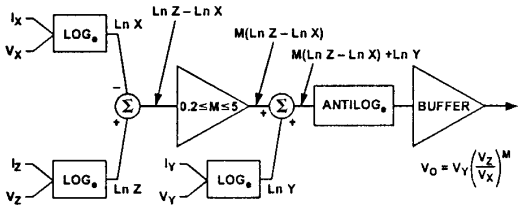


Figure 10. Model Circuit

USING THE VOLTAGE REFERENCES

A stable bandgap voltage reference for scaling is included in the AD538. It is laser-trimmed to provide a selectable voltage output of +10 V buffered (Pin 4), +2 V unbuffered (Pin 5) or any voltages between +2 V and +10.2 V buffered as shown in Figure 11. The output impedance at Pin 5 is approximately 5 kΩ. Note that any loading of this pin will produce an error in the +10 V reference voltage. External loads on the +2 V output should be greater than 500 kΩ to maintain errors less than 1%.

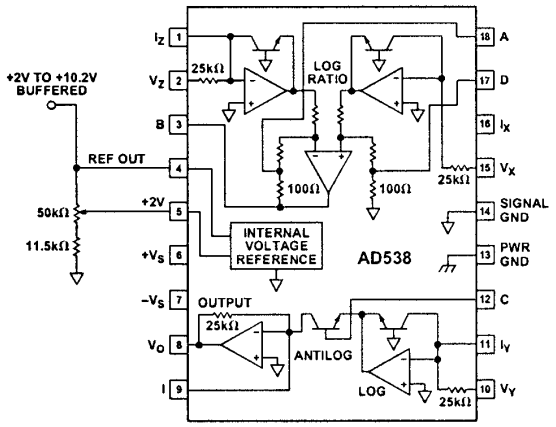


Figure 11. +2 V to +10.2 V Adjustable Reference

In situations not requiring both reference levels, the +2 V output can be converted to a buffered output by tying Pins 4 and 5 together. If both references are required simultaneously, the +10 V output should be used directly and the +2 V output should be externally buffered.

ONE-QUADRANT MULTIPLICATION/DIVISION

Figure 12 shows how the AD538 may be easily configured as a precision one-quadrant multiplier/divider. The transfer function $V_{OUT} = V_Y (V_Z/V_X)$ allows "three" independent input variables, a calculation not available with a conventional multiplier. In addition, the 1000:1 (i.e., 10 mV to 10 V) input dynamic range of the AD538 greatly exceeds that of analog multipliers computing one-quadrant multiplication and division.

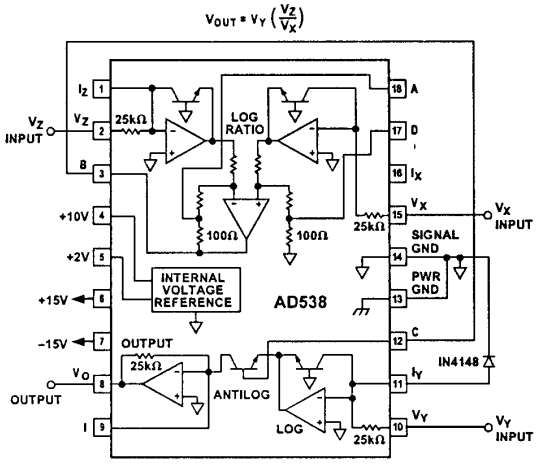


Figure 12. One-Quadrant Combination Multiplier/Divider

By simply connecting the input V_X (Pin 15) to the +10 V reference (Pin 4), and tying the log-ratio output at B to the antilog input at C, the AD538 can be configured as a one-quadrant analog multiplier with 10-volt scaling. If 2-volt scaling is desired, V_X can be tied to the +2 V reference.

When the input V_X is tied to the +10 V reference terminal, the multiplier transfer function becomes:

$$V_O = V_Y \left(\frac{V_Z}{10\ V}\right)$$

As a multiplier, this circuit provides a typical bandwidth of 400 kHz with values of V_X, V_Y or V_Z varying over a 100:1 range (i.e., 100 mV to 10 V). The maximum error with a 100 mV to 10 V range for the two input variables will typically be +0.5% of reading. Using the optional Z offset trim scheme, as shown in Figure 13, this error can be reduced to +0.25% of reading.

By using the +10 V reference as the V_Y input, the circuit of Figure 12 is configured as a one-quadrant divider with a fixed scale factor. As with the one-quadrant multiplier, the inputs accept only single (positive) polarity signals. The output of the one-quadrant divider with a +10 V scale factor is:

$$V_O = 10\ V \left(\frac{V_Z}{V_X}\right)$$

The typical bandwidth of this circuit is 370 kHz with 1 V to 10 V denominator input levels. At lower amplitudes, the bandwidth gradually decreases to approximately 200 kHz at the 2 mV input level.

AD538

TWO-QUADRANT DIVISION

The two-quadrant linear divider circuit illustrated in Figure 13 uses the same basic connections as the one-quadrant version. However, in this circuit the numerator has been offset in the positive direction by adding the denominator input voltage to it. The offsetting scheme changes the divider's transfer function from:

$$V_O = 10V\left(\frac{V_Z}{V_X}\right)$$

to:

$$V_O = 10V\frac{(V_Z + AV_X)}{V_X} = 10V\left(1A + \frac{V_Z}{V_X}\right)$$

$$= 10A + 10V\left(\frac{V_Z}{V_X}\right)$$

where $A = \left(\frac{35\,k\Omega}{25\,k\Omega}\right)$

As long as the magnitude of the denominator input is equal to or greater than the magnitude of the numerator input, the circuit will accept bipolar numerator voltages. However, under the conditions of a 0 V numerator input, the output would incorrectly equal +14 V. The offset can be removed by connecting the +10 V reference through resistors R1 and R2 to the output section's summing node I at Pin 9 thus providing a gain of 1.4 at the center of the trimming potentiometer. The pot R2 adjusts out or corrects this offset, leaving the desired transfer function of 10 V (V_Z/V_X).

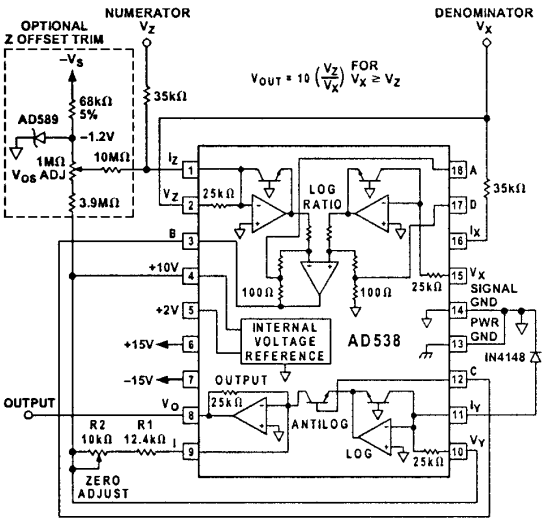


Figure 13. Two-Quadrant Division with 10 V Scaling

LOG RATIO OPERATION

Figure 14 shows the AD538 configured for computing the log of the ratio of two input voltages (or currents). The output signal from B is connected to the summing junction of the output amplifier via two series resistors. The 90.9 Ω metal film resistor effectively degrades the temperature coefficient of the ±3500 ppm/°C resistor to produce a 1.09 kΩ +3300 ppm/°C equivalent value. In this configuration, the V_Y input must be tied to some voltage less than zero (−1.2 V in this case) removing this input from the transfer function.

The 5 kΩ potentiometer controls the circuit's scale factor adjustment providing a +1 V per decade adjustment. The output offset potentiometer should be set to provide a zero output with $V_X = V_Z = 1$ V. The input V_Z adjustment should be set for an output of 3 V with $V_Z = 1$ mV and $V_X = 1$ V.

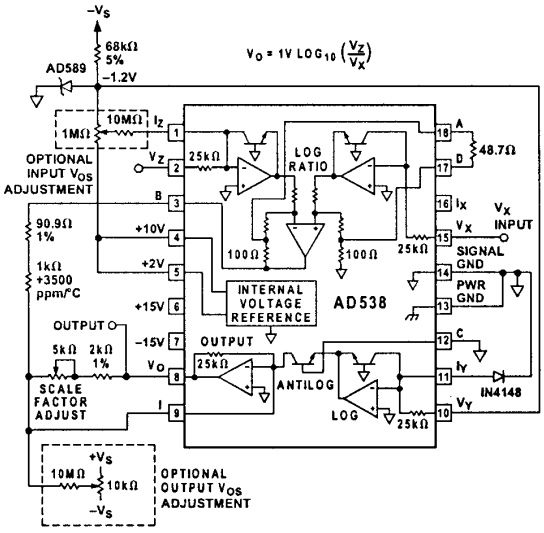


Figure 14. Log Ratio Circuit

The log ratio circuit shown achieves ±0.5% accuracy in the log domain for input voltages within three decades of input range: 10 mV to 10 V. This error is not defined as a percent of full-scale output, but as a percent of input. For example, using a 1 V/decade scale factor, a 1% error in the positive direction at the INPUT of the log ratio amplifier translates into a 4.3 mV deviation from the ideal OUTPUT (i.e., 1 V × $\log_{10}$ (1.01) = 4.3214 mV). An input error 1% in the negative direction is slightly different, giving an output deviation of 4.3648 mV.

ANALOG COMPUTATION OF POWERS AND ROOTS

It is often necessary to raise the quotient of two input signals to a power or take a root. This could be squaring, cubing, square-rooting or exponentiation to some noninteger power. Examples include power series generation. With the AD538, only one or two external resistors are required to set ANY desired power, over the range of 0.2 to 5. Raising the basic quantity V_Z/V_X to a power greater than one requires that the gain of the AD538's log ratio subtractor be increased, via an external resistor between pins A and D. Similarly, a voltage divider that attenuates the log ratio output between points B and C will program the power to a value less than one.

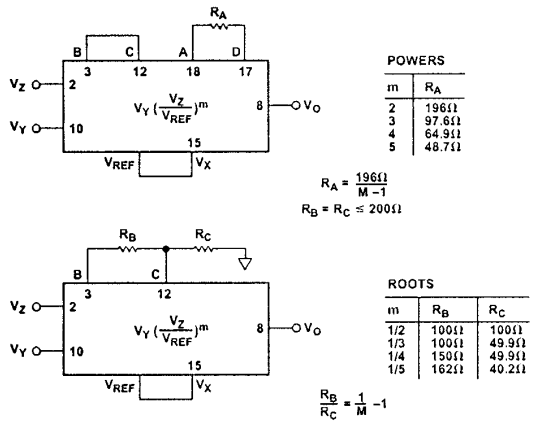


Figure 15. Basic Configurations and Transfer Functions for the AD538

SQUARE ROOT OPERATION

The explicit square root circuit of Figure 16 illustrates a precise method for performing a real-time square root computation. For added flexibility and accuracy, this circuit has a scale factor adjustment.

The actual square rooting operation is performed in this circuit by raising the quantity V_Z/V_X to the one-half power via the resistor divider network consisting of resistors R_B and R_C. For maximum linearity, the two resistors should be 1% (or better) ratio-matched metal film types.

One volt scaling is achieved by dividing-down the 2 V reference and applying approximately 1 V to both the V_Y and V_X inputs. In this circuit, the V_X input is intentionally set low, to about 0.95 V, so that the V_Y input can be adjusted high, permitting a ±5% scale factor trim. Using this trim scheme, the output voltage will be within ±3 mV ± 0.2% of the ideal value over a 10 V to 1 mV input range (80 dB). For a decreased input dynamic range of 10 mV to 10 V (60 dB) the error is even less; here the output will be within ±2 mV ± 0.2% of the ideal value. The bandwidth of the AD538 square root circuit is approximately 280 kHz with a 1 V p-p sine wave with a +2 V dc offset.

This basic circuit may also be used to compute the cube, fourth or fifth roots of an input waveform. All that is required for a given root is that the correct ratio of resistors, R_C and R_B, be selected such that their sum is between 150Ω and 200Ω.

The optional absolute value circuit shown preceding the AD538 allows the use of bipolar input voltages. Only one op amp is required for the absolute value function because the I_Z input of the AD538 functions as a summing junction. If it is necessary to preserve the sign of the input voltage, the polarity of the op amp output may be sensed and used after the computation to switch the sign bit of a D.V.M. chip.

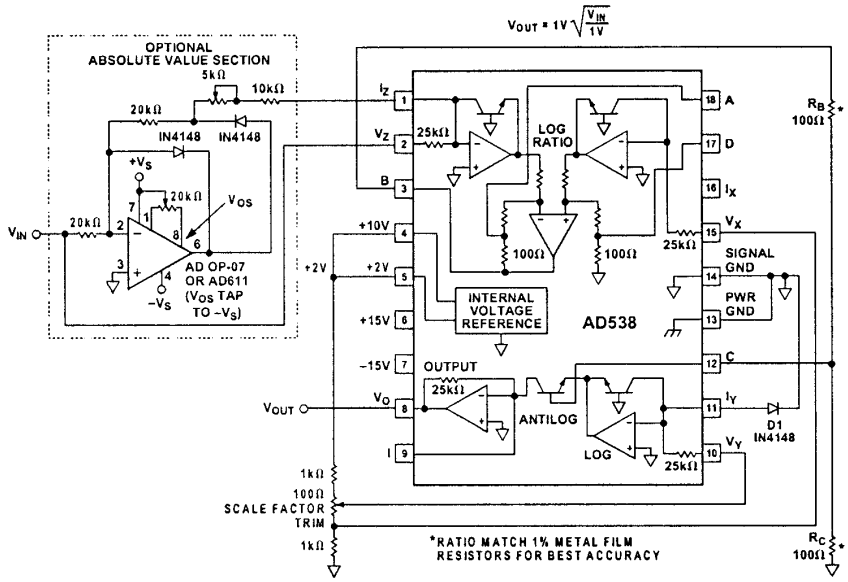


Figure 16. Square Root Circuit

PRELIMINARY

DG271
High Speed Quad Monolithic SPST CMOS Analog Switch

Siliconix

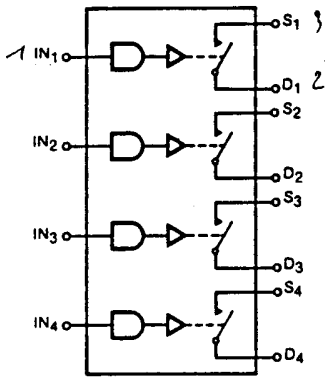
FEATURES	BENEFITS	APPLICATIONS
• Fast Switching Times <75 ns	• Faster System Operation	• High Speed Switching
• Power Dissipation <157 mW	• Reduced Power Supply Requirements	• Sample/Hold
• Charge Injection <9.0 pC	• Reduced System Error	• Digital Filters
• rDS(on) <50 Ω	• Pull-up Resistors not Required	• Op Amp Gain Switching
• TTL Compatible		• Winchester Disk Drives

DESCRIPTION

The DG271 Quad SPST analog switch offers normally open, high speed break-before-make switching for applications where low ON resistance (32 Ω typ), wide signal range (±15 V), and low charge-transfer are required. In the OFF state, the switch will block up to 30 V peak-to-peak, and has a 44 V maximum power supply rating. The DG271 will conduct current in either direction with no offset in the ON state. ON resistance is nearly constant over the entire analog signal range, thus providing precision signal transfer across the switch. Internal pull-up resistors simplify interface to CMOS or TTL drive circuits. Package options are 16 pin plastic or ceramic DIP, with performance rated over the 0 to 70°C and −25 to 85°C temperature ranges.

2

FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches per Package*

Truth Table

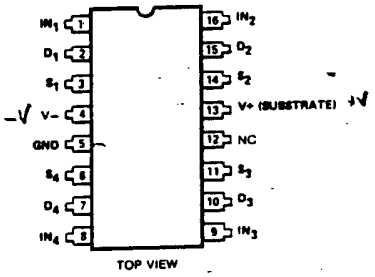
LOGIC	SWITCH
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION

Dual-In-Line Package



Order Numbers:
DG271BK or DG271CK
See Package 10

DG271CJ
See Package 8

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[1] V_S, V_D ..... −2 V to (V^+ +2 V) or 20 mA, whichever occurs first.
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 msec. 10% duty cycle max) ..... 100 mA
Storage Temperature (B Suffix) .....−65 to 150°C
(C Suffix) .....−65 to 125°C
Operating Temperature (B Suffix) .....−25 to 85°C
(C Suffix) ..... 0 to 70°C
Power Dissipation (Package)*
16 Pin DIP** ..... 900 mW
16 Pin Plastic DIP*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS[2]

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V− = −15 V, GND = 0		LIMITS MIN[3]	LIMITS TYP[4]	LIMITS MAX	UNIT
SWITCH	Analog Signal Range	V_{ANALOG}			−15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA, V_{in} = 0.8 V			32	50	Ω
	Source OFF Leakage Current	$I_{S(off)}$	V_{in} = 2.0 V	V_S = 14 V, V_D = −14 V			1	nA
				V_S = −14 V, V_D = 14 V	−1			
	Drain OFF Leakage Current	$I_{D(off)}$		V_S = −14 V, V_D = 14 V			1	
				V_S = 14 V, V_D = −14 V	−1			
	Drain ON Leakage Current[5]	$I_{D(on)}$	V_{in} = 0.8 V	V_S = V_D = 14 V			1	
				V_S = V_D = −14 V	−1			
INPUT	Input Current with Input Voltage High	I_{INH}	V_{in} = 2.0 V		−1	0.22		µA
			V_{in} = 15 V			0.035	1	
	Input Current with Input Voltage Low	I_{INL}	V_{in} = 0 V		−1	0.010		
DYN	Turn-ON Time	t_{on}	See Switching Time Test Circuit			53.0	75	ns
	Turn-OFF Time	t_{off}				50.6	75	
	Charge Injection[6]	Q	C_L = 1000pF, V_{gen} = 0 V, R_{gen} = 0 Ω			9.0		pC
SUPPLY	Positive Supply Current	I^+	All Channels "ON" or "OFF" V_{in} = 0 or 2 V			4.3	6.0	mA
	Negative Supply Current	I^-			−4.5	−3.4		

T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V− = −15 V, GND = 0		LIMITS MIN[3]	LIMITS TYP[4]	LIMITS MAX	UNIT
SWITCH	Analog Signal Range	V_{ANALOG}	V_D = ±10 V, I_S = 1 mA, V_{in} = 0.8 V		−15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10 V I_S = 1 mA V_{in} = 0.8 V				75	Ω
	Source OFF Leakage Current	$I_{S(off)}$	V_{in} = 2.0 V	V_S = 14 V, V_D = −14 V			100	nA
				V_S = −14 V, V_D = 14 V	−100			
	Drain OFF Leakage Current	$I_{D(off)}$		V_S = −14 V, V_D = 14 V			100	
				V_S = 14 V, V_D = −14 V	−100			
	Drain ON Leakage Current[5]	$I_{D(on)}$	V_{in} = 0.8 V	V_S = V_D = 14 V			200	
				V_S = V_D = −14 V	−200			
INPUT	Input Current with Input Voltage High	I_{INH}	V_{in} = 2.0 V		−10			µA
			V_{in} = 15 V				10	
	Input Current with Input Voltage Low	I_{INL}	V_{in} = 0 V		−10			

NOTES:
1. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART For additional information.
3. The algebraic convention whereby the most negative value is minimum, and the most positive is maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. $I_{D(on)}$ is leakage from driver into "ON" switch.

ANALOG DEVICES

Very Fast, Complete 10- or 12-Bit A/D Converters

AD578/AD579

FEATURES

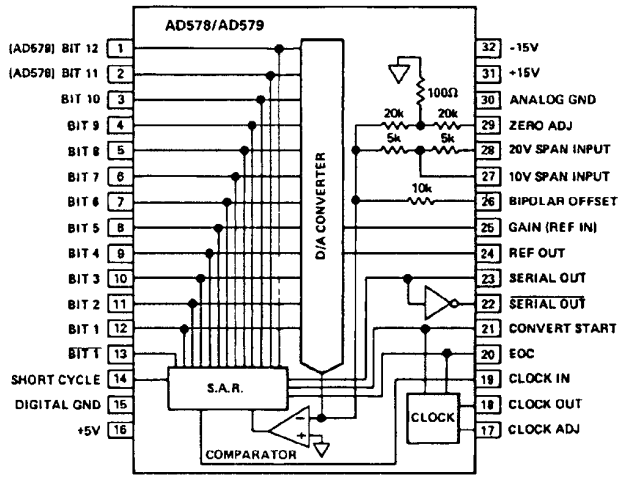
Performance

- Complete 12-Bit A/D Converter with Reference and Clock
- Fast Conversion: 3 μs (max)
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30 ppm/°C max (AD578)
  ±40 ppm/°C max (AD579)
- Max Nonlinearity: <±0.012%
- No Missing Codes Over Temperature
- Low Power: 555 mW (AD578); 775 mW (AD579)
- Available to MIL-STD-883

Versatility

- Positive-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +10 V Reference for External Applications
- Adjustable Internal Clock
- "Z" Models for ±12 V Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD578 and AD579 are high speed 12-bit and 10-bit successive approximation analog-to-digital converters that include internal clock, reference, and comparator. Their hybrid design utilizes MSI digital and linear ICs in conjunction with a 12-bit or 10-bit monolithic, monotonic DAC to provide superior performance and versatility with IC size, price, and reliability.

Important performance characteristics of the AD578 include ±1/2 LSB_{12} linearity error maximum at +25°C, maximum gain tempco of ±30 ppm/°C, and maximum conversion time of 3 μs at a typical power dissipation of 555 mW. The 10-bit AD579 provides ±1/2 LSB_{10} maximum linearity error at 1.8 μs maximum, and 775 mW typical P_D.

Both the AD578 and AD579 include scaling resistors that provide analog input signal ranges of ±5 V, ±10 V, and 0 to +10 V. Both are contained in 32-pin ceramic side-brazed DIP packages, and are available with MIL-STD-883 Class B processing.

PRODUCT HIGHLIGHTS

1. Both are complete analog-to-digital converters. No external components are required to perform a conversion.
2. The fast conversion rates—3 μs for the AD578, and 1.8 μs for the AD579—make them ideal candidates for high speed data acquisition systems requiring high throughput.
3. The internal buried Zener reference is laser trimmed to high initial accuracy and low T.C. and is available externally.
4. Precision thin film scaling resistors on the DAC provide for excellent thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolution.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD578/AD579—SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Model	AD578J	AD578K	AD578L	AD578SD[1]	AD578TD[1]
RESOLUTION	12 Bits	*	*	*	*
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±5.0 V, ±10 V	*	*	*	*
Unipolar	0 to +10 V, 0 to +20 V	*	*	*	*
Input Impedance					
0 to +10 V, ±5 V	5 kΩ	*	*	*	*
±10 V, 0 to +20 V	10 kΩ	*	*	*	*
DIGITAL INPUTS					
Convert Command[2]	1 LSTTL Load	*	*	*	*
Clock Input	1 LSTTL Load	*	*	*	*
TRANSFER CHARACTERISTICS					
Gain Error[3, 4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Unipolar Offset[4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Bipolar Error[4, 5]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Linearity Error, +25°C	±1/2 LSB max	*	*	*	*
T_{min} to T_{max}	±3/4 LSB	*	*	±3/4 LSB max	±3/4 LSB max
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)					
+25°C	12 Bits	*	*	*	*
T_{min} to T_{max}	12 Bits	*	*	*	*
POWER SUPPLY SENSITIVITY					
+15 V ±10%	0.005%/%ΔV_S max	*	*	*	*
−15 V ±10%	0.005%/%ΔV_S max	*	*	*	*
+5 V ±10%	0.005%/%ΔV_S max	*	*	*	*
TEMPERATURE COEFFICIENTS					
Gain	±15 ppm/°C typ	*	*	*	*
	±30 ppm/°C max	*	*	±50 ppm/°C max	±30 ppm/°C max
Unipolar Offset	±3 ppm/°C typ	*	*	*	*
	±10 ppm/°C max	*	*	±15 ppm/°C max	±10 ppm/°C max
Bipolar Offset	±8 ppm/°C typ	*	*	*	*
	±20 ppm/°C max	*	*	±25 ppm/°C max	±20 ppm/°C max
Differential Linearity	±2 ppm/°C typ	*	*	*	*
CONVERSION TIME[6, 7, 8] (max)	6.0 µs	4.5 µs	3 µs	6.0 µs	4.5 µs
PARALLEL OUTPUTS					
Unipolar Code	Binary	*	*	*	*
Bipolar Code	Offset Binary/Twos Complement	*	*	*	*
Output Drive	2 LSTTL Loads	*	*	*	*
SERIAL OUTPUTS (NRZ FORMAT)					
Unipolar Code	Binary/Complementary Binary	*	*	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*	*	*
Output Drive	2 LSTTL Loads	*	*	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*	*	*
Output Drive	8 LSTTL Loads	*	*	*	*
INTERNAL CLOCK[8]					
Output Drive	2 LSTTL Loads	*	*	*	*
INTERNAL REFERENCE					
Voltage	10.000 ±100 mV	*	*	*	*
Drift	±12 ppm/°C, ±20 ppm/°C max	*	*	*	*
External Current	±1 mA max	*	*	*	*
POWER SUPPLY REQUIREMENTS[9]					
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	*
Supply Current +15 V	5 mA typ, 8 mA max	*	*	*	*
−15 V	22 mA typ, 35 mA max	*	*	*	*
+5 V	30 mA typ, 40 mA max	*	*	*	*
Power Dissipation	555 mW typ	*	*	*	*
TEMPERATURE RANGE					
Operating	0 to +70°C	*	*	−55°C to +125°C	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*	*

NOTES
[1]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.
[2]Positive pulse 200 ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.
[3]With 50 Ω, 1% fixed resistor in place of gain adjust potentiometer.
[4]Adjustable to zero.
[5]With 50 Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).
[6]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.
[7]Each grade is specified at the conversion speed shown.
[8]Externally adjustable by a resistor or capacitor (see Figure 6).
[9]For "Z" models order AD578ZJ, ZK, ZL (±11.6 V to ±16.5 V).
*Specifications same as AD578J.
Specifications subject to change without notice.

Model	AD579JN	AD579KN	AD579TD[1]
RESOLUTION	10 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0 V, ±10 V	*	*
Unipolar	0 to +10 V, 0 to +20 V	*	*
Input Impedance			
0 to +10 V, ±5 V	5 kΩ (±20%)	*	*
±10 V, 0 to +20 V	10 kΩ (±20%)	*	*
DIGITAL INPUTS			
Convert Command[2]	1 LSTTL Load	*	*
Clock Input	1 LSTTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error[3, 4]	±0.1% FSR (±0.25% FSR max)	*	*
Unipolar Offset[3]	±0.1% FSR (±0.25% FSR max)	*	*
Bipolar Error[3, 4]	±0.1% FSR (±0.25% FSR max)	*	*
Linearity Error, +25°C	±1/2 LSB max	*	*
T_{min} to T_{max}	±3/4 LSB	*	*
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	10 Bits	*	*
POWER SUPPLY SENSITIVITY			
+15 V ±10%	0.005%/%ΔV_S max	*	*
−15 V ±10%	0.005%/%ΔV_S max	*	*
+5 V ±10%	0.001%/%ΔV_S max	*	*
"Z" Versions			
+12 V ±5%	0.007%/%ΔV_S max	*	*
−12 V ±5%	0.007%/%ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	±25 ppm/°C typ	*	*
	±40 ppm/°C max	*	*
Unipolar Offset	±5 ppm/°C typ	*	*
	±15 ppm/°C max	*	*
Bipolar Offset	±8 ppm/°C typ	*	*
	±20 ppm/°C max	*	*
Differential Linearity	±2 ppm/°C typ	*	*
CONVERSION TIME[3, 6] (max)	2.2 µs	1.8 µs	**
Conversion Time T_{min} to T_{max}	2.4 µs	2.0 µs	**
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Twos Complement	*	*
Output Drive	2 LSTTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive	2 LSTTL Loads	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*
Output Drive	8 LSTTL Loads	*	*
INTERNAL CLOCK[7]			
Output Drive	2 LSTTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 ±10 mV typ	*	*
Temperature Coefficient	15 ppm/°C	*	*
External Current	±1 mA max	*	*
POWER SUPPLY REQUIREMENTS			
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*
Supply Current +15 V	5 mA typ, 8 mA max	*	*
−15 V	22 mA typ, 35 mA max	*	*
+5 V	100 mA typ, 150 mA max	*	*
Power Dissipation	775 mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

NOTES
[1]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.
[2]Positive pulse 200 ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.
[3]With 50 Ω, 1% fixed resistor in place of gain adjust potentiometer.
[4]Adjustable to zero.
[5]With 50 Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).
[6]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.
[7]Each grade is specified at the conversion speed shown. See Figure 7 for appropriate connections.
[8]Externally adjustable by a resistor or capacitor.
[9]For "Z" models order AD579ZJN, AD579ZKN or AD579ZTD.
*Specifications same as AD579JN.
**Specifications same as AD579KN.
Specifications subject to change without notice.

Tournez la page S.V.P.

AD578/AD579

ORDERING GUIDE[1]

Model	Resolution	Conversion Speed	Temperature Range	Package Option[2]
AD578JN (JD)	12 Bits	6.0 µs	0°C to +70°C	DH-32B
AD578KN (KD)	12 Bits	4.5 µs	0°C to +70°C	DH-32B
AD578LN (LD)	12 Bits	3.0 µs	0°C to +70°C	DH-32B
AD578SD	12 Bits	6.0 µs	−55°C to +125°C	DH-32B
AD578TD	12 Bits	4.5 µs	−55°C to +125°C	DH-32B
AD578SD/883B	12 Bits	6.0 µs	−55°C to +125°C	DH-32B
AD578TD/883B	12 Bits	4.5 µs	−55°C to +125°C	DH-32B
AD579JN	10 Bits	2.2 µs	0°C to +70°C	DH-32B
AD579KN	10 Bits	1.8 µs	0°C to +70°C	DH-32B
AD579TD	10 Bits	1.8 µs	−55°C to +125°C	DH-32B
AD579TD/883B	10 Bits	1.8 µs	−55°C to +125°C	DH-32B

NOTES
[1]For ±12 V operation "Z" Version, order AD578ZTD

THEORY OF OPERATION

The AD578 is a complete pretrimmed 12-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD578 is shown in Figure 1.

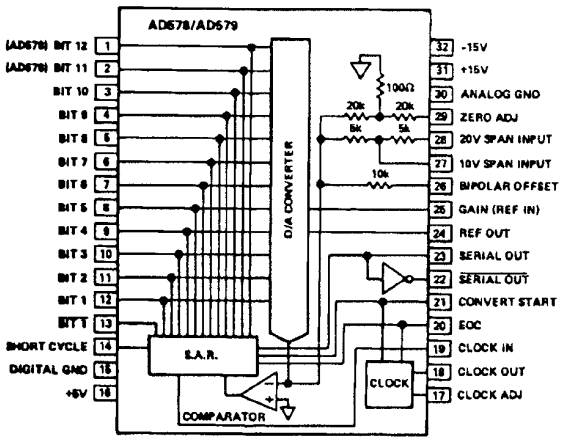
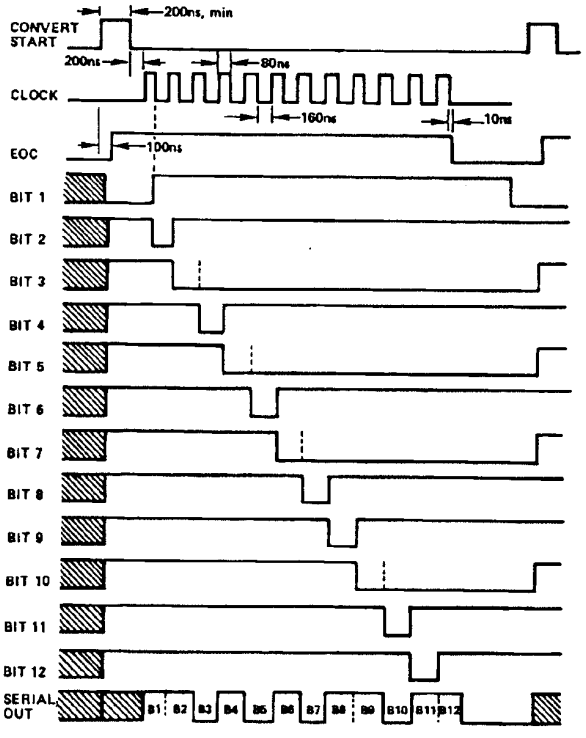


Figure 1. AD578/AD579 Functional Block Diagram and Pinout

When the control section is commanded to initiate a conversion it enables the clock and resets the successive-approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The data bits are valid on the falling edge of the clock pulse starting with t_1 and ending with t_{12} (Figure 2), and accurately represent the input signal to within ±1/2 LSB.



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
[1]THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 2a. AD578 3 µs Timing Diagram

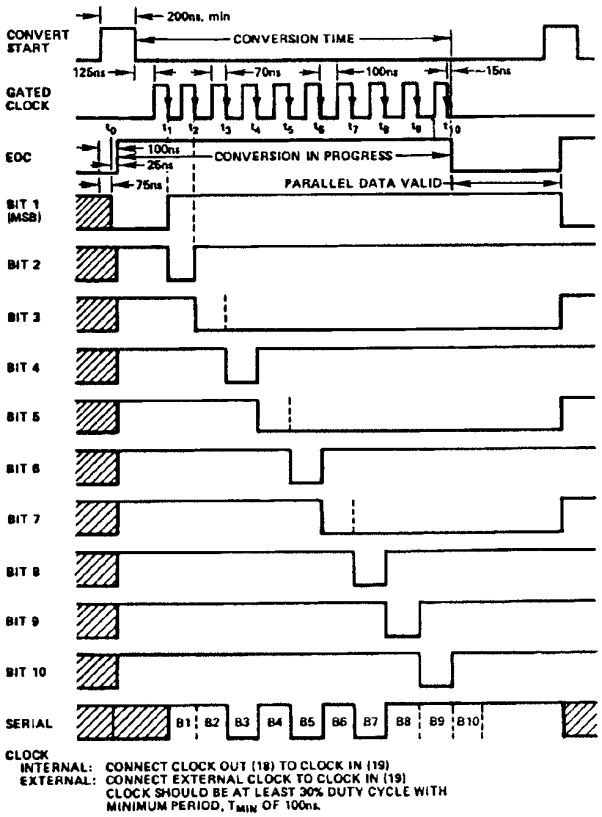


Figure 2b. AD579 Timing Diagram

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1.0%, it is buffered and can supply up to 1.0 mA to an external load in addition to the current required to drive the reference input resistor (0.5 mA) and bipolar offset resistor (1 mA). The thin-film application resistors are trimmed to match the full scale output current of the DAC. There are two 5 kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10 kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578/AD579 is intended to have a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB.

If Pin 26 is connected to Pin 30, the unit will behave in this manner, within specifications. Refer to Table I, Table II, and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±25 mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale. Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

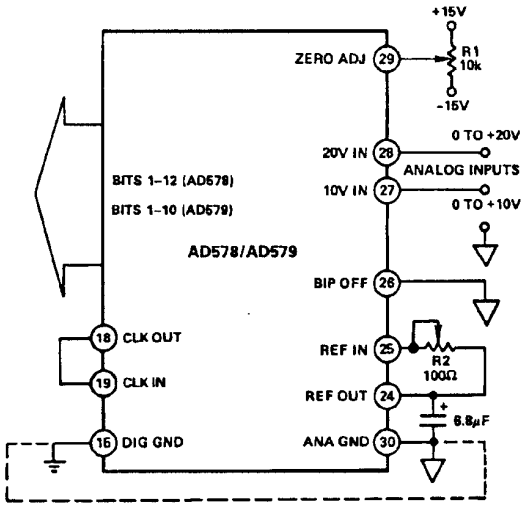


Figure 3. Unipolar Input Connections

Table I. AD578 Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input–Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10 V Range	0 to +20 V Range	−5 V to +5 V Range	−10 V to +10 V Range	B1 (MSB)	B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1	
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0	
•	•	•	•	•	
•	•	•	•	•	
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1	
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0	
•	•	•	•	•	
•	•	•	•	•	
+0.0024	+0.0051	−4.9976	−9.9951	0 0 0 0 0 0 0 0 0 0 0 1	
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0	

Table II. AD579 Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input–Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10 V Range	0 to +20 V Range	−5 V to +5 V Range	−10 V to +10 V Range	B1 (MSB) B12 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1 1 1 1 1 1 1 1 1 1 1 1
+9.9804	+19.9609	+4.9804	+9.9609	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0097	+10.0195	+0.0097	+0.0195	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0097	+0.0195	−4.9902	−9.9804	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient the 100 Ω trimmer shown can be replaced by a 50 Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). The a signal 1 1/2 LSB below positive full scale is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

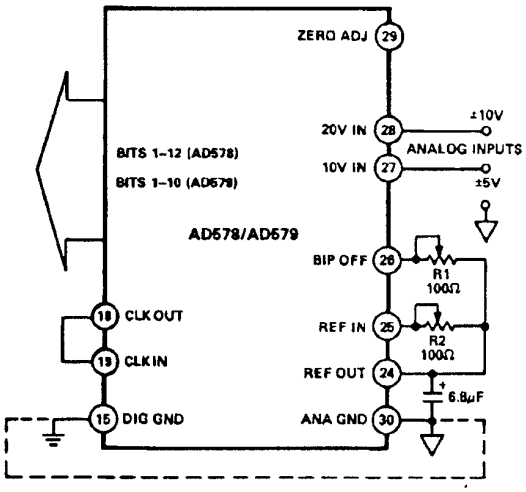


Figure 4. Bipolar Input Connections

LAYOUT CONSIDERATION

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578 or AD579. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

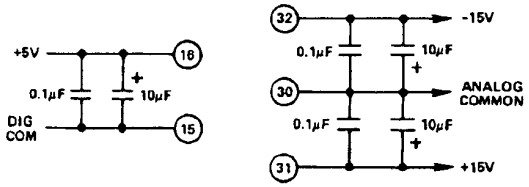


Figure 5. Basic Bypassing Practice

Each of the AD578 or AD579 supply terminals should be capacitively decoupled as close to the ADC as possible. A large value capacitor such as 10 μF in parallel with a 0.1 μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

To minimize noise the reference output (Pin 24) should be decoupled by a 6.8 μF capacitor to Pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 5.6 μs (AD578) or 4.8 μs (AD579). It can be adjusted for either faster or slower conversion rates. For faster conversions connect the appropriate 1% resistor between Pins 17 and 18, and short Pin 18 to Pin 19. See Figure 6 or 7.

For slower conversions (AD578 only) connect a capacitor between Pins 15 and 17.

NOTE: No-Missing-Code operation is not guaranteed when operating in this mode if a particular grade's conversion speed specification is exceeded.

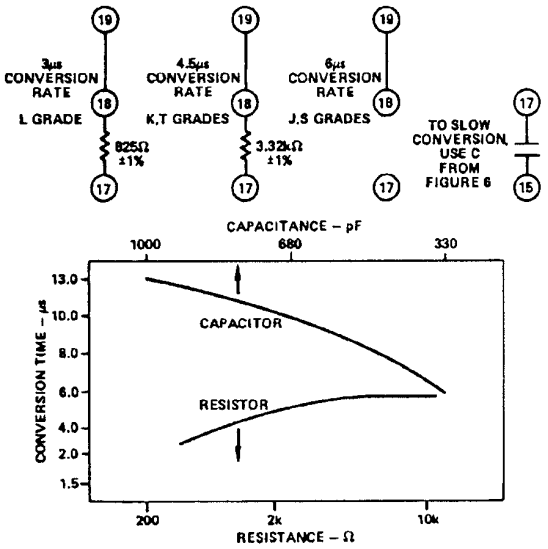


Figure 6. AD578 Conversion Times vs. R or C Values

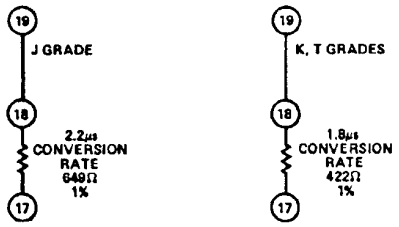


Figure 7. AD579 Clock Rate Control Connection

Short Cycle Input—A short cycle input, Pin 14, permits the timing cycle to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring the full 10-bit (AD579) or 12-bit (AD578) resolution. Short cycle pin connections and associated conversion times are summarized in Tables III and IV.

Table III. AD578 Short Cycle Connections

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	3	2.5	2

Table IV. AD579 Short Cycle Connections

Resolution (Bits)	10	8
Connect Pin 14 to Pin	2	4
Conversion Speed (μs)	1.8	1.5

External Clock—An external clock may be connected directly to the clock input, Pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier—In applications where the AD578 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD711 should be used.

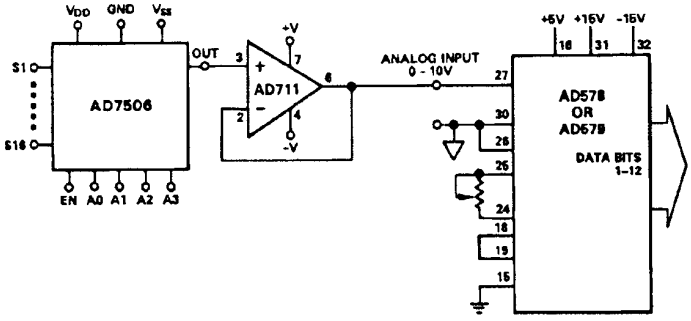


Figure 8. Input Buffer

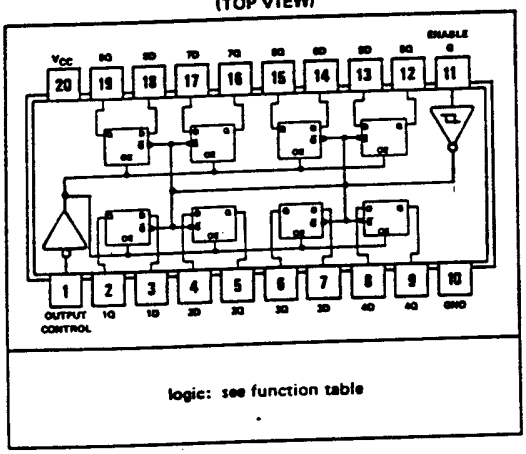
TTL
MSI

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7612350, OCTOBER 1976

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)
- SN54LS363 and SN74LS364 Are Similar But Have Higher V_{OH} For MOS Interface

SN54LS373, SN54S373 . . . J PACKAGE
SN74LS373, SN74S373 . . . J OR N PACKAGE
(TOP VIEW)

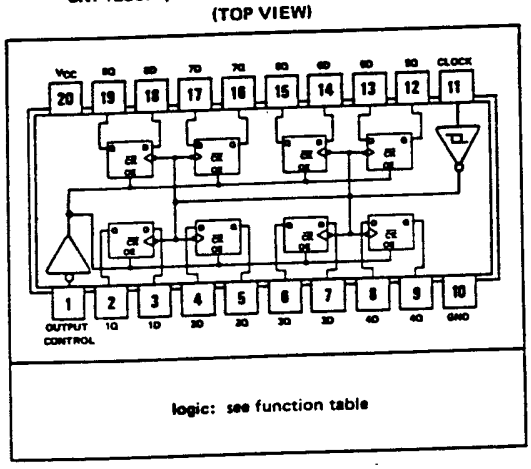


logic: see function table

'LS373, 'S373
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS374, SN54S374 . . . J PACKAGE
SN74LS374, SN74S374 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

'LS374, 'S374
FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

See explanation of function tables on page 3-8.

description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

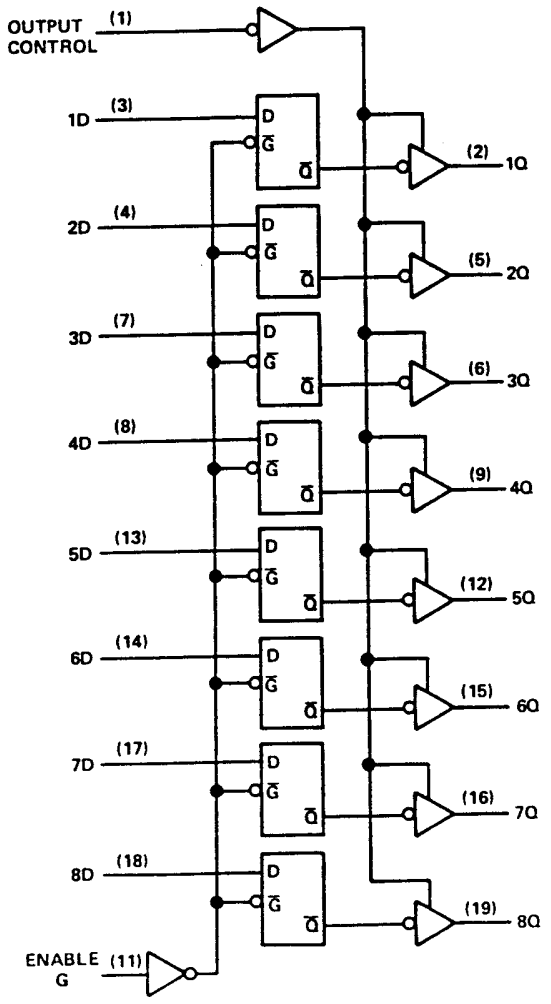
description (continued)

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

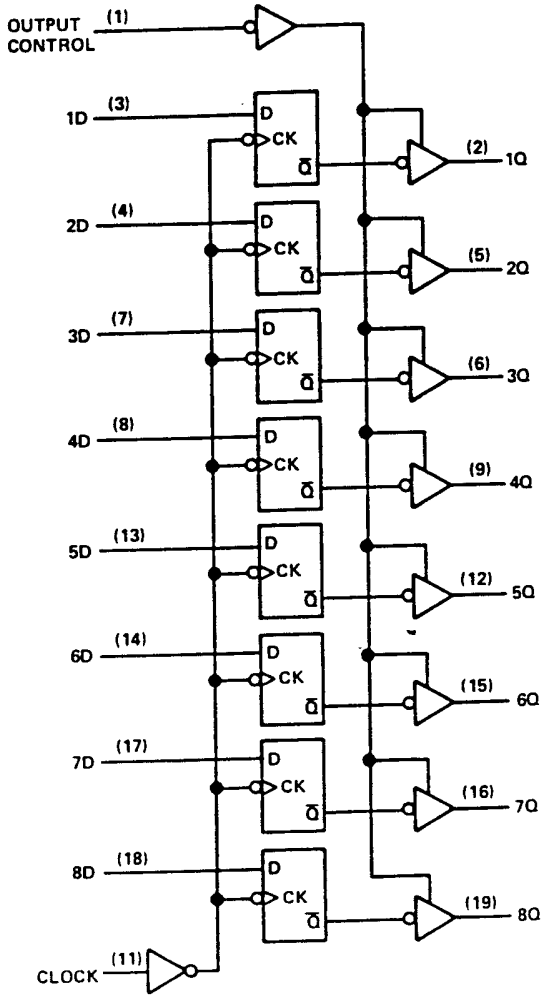
Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

'LS373, 'S373
TRANSPARENT LATCHES



'LS374, 'S374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

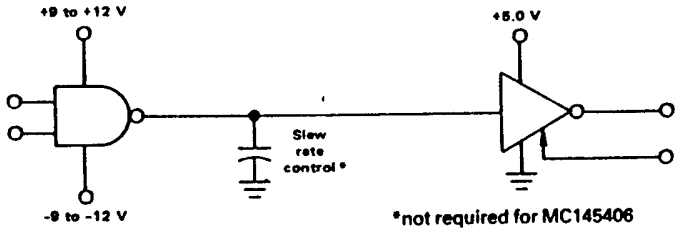


RS-232C DATA COMMUNICATIONS

EIA Standard RS-232C is an established specification defining the logic levels and impedances at the modem/terminal interface. This has been a well-accepted standard for low data-rate systems. Maximum data rate is about 20 kilobaud.

Employing a voltage-mode type driver, RS-232C requires dual polarity logic signals and power supplies. The data is unidirectional and not conducive to party-line operation. Hysteresis is generally employed in RS-232C receivers and a single power supply is required at the receiver end. Termination is not required.

FIGURE 6



*not required for MC145406

EIA RS-232C	
Driver Output Voltage (Z_L = 3 kΩ to 7 kΩ)	$15\ V \leq V_{OH} \leq 5.0\ V$ $-5.0\ V \geq V_{OL} \geq -15\ V$
Driver Output Voltage (Z_L = ∞)	$\lvert V_O \rvert < 25\ V$
Driver Output Impedance (Power Supplies = 0)	$Z_O > 300\ \Omega$
Driver Short-Circuit Current	$\lvert I_O \rvert < 0.5$ amp
Driver Slew Rate	$\frac{dv}{dt} < 30\ V/\mu s$
Receiver Input Impedance	$7\ k\Omega > R_{in} > 3\ k\Omega$
Receiver Input Voltage	$V_I < 25\ V$
Receiver Output with Open Input	Mark (high)
Receiver Output with 300 Ω to Gnd of Input	Mark (high)
Receiver Output with +3.0 V on Input	Space (low)
Receiver Output with -3.0 V on Input	Mark (high)
Baud Rate	BR ≤ 20 kilobaud

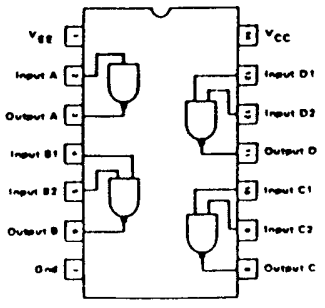
MC1488 - QUAD RS-232C DRIVER, OUTPUT CURRENT LIMITING

The MC1488 is a quad inverting TTL or DTL input line driver for RS-232C. It is designed to operate on ±9 to ±12 V power supplies and at a temperature range of 0 to 70°C.

Features include guaranteed power-off output impedance and output current limiting.

Packages: L Suffix - Case 632
P Suffix - Case 646
D Suffix - Case 751A

Second sources available



V_{OH} @ V_{CC}/V_{EE} = ±9.0 V Volts Min	V_{OL} @ V_{CC}/V_{EE} = ±9.0 V Volts Max	I_{OS} mA	t_{PHL} @ C_L = 15 pF ns Max
6.0	-6.0	±6.0 to 12	175

HEWLETT PACKARD

COMPOSANTS

EMETTEUR A BOUCLE DE COURANT 20 mA A COUPLAGE OPTIQUE

HCPL-4100

FICHE TECHNIQUE JANVIER 1986

SCHEMA

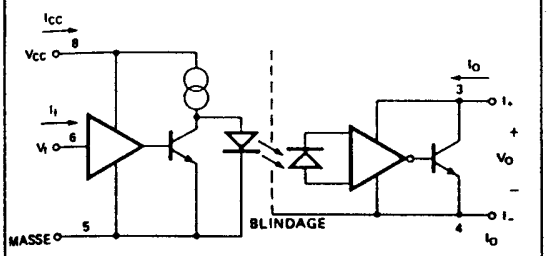
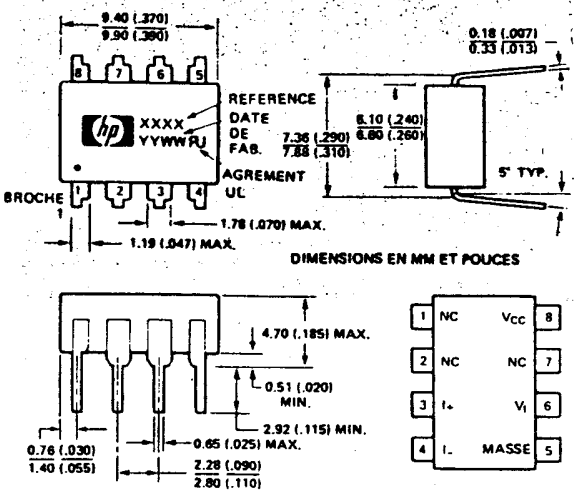


TABLEAU DE VERITE (LOGIQUE POSITIVE)*

V_I	V_{CC}	I_O
H	1	H
L	1	L
H	0	H
L	0	H

* CONVENTION DE LA BOUCLE DE COURANT - H = SIGNAL : I_O > 12 mA, L = ESPACE : I_O < 2 mA.

BOITIER*



DIMENSIONS EN MM ET POUCES

Caractéristiques

- BOUCLE DE COURANT 20 mA A PARAMETRES GARANTIS
- ENTREE DES DONNEES COMPATIBLES LSTTL, TTL ET CMOS
- PERFORMANCES GARANTIES ENTRE 0°C ET 70°C
- BLINDAGE INTERNE FAVORISANT UNE TRES BONNE REJECTION EN MODE COMMUN
- VITESSE DE TRANSMISSION : 20 kBd SUR UNE LIGNE DE 400 METRES
- NIVEAUX DE COURANT DE SORTIE EN/HORS GARANTIS
- AGREE UL (DOSSIER N° E55361) POUR UNE TENSION D'ISOLEMENT DE 1440 Vca/1 mn ET DE 2500 Vca/1 mn (OPTION 010)
- EGALEMENT DISPONIBLE : RECEPTEUR A BOUCLE DE COURANT 20 mA A COUPLAGE OPTIQUE, HCPL-4200

Applications

- MISE EN OEUVRE D'UN EMETTEUR ISOLE A BOUCLE DE COURANT 20 mA DANS :
  - les périphériques de systèmes informatiques
  - l'équipement de commande industriel
  - l'équipement de transmission de données

Description

Le photocoupleur HCPL-4100 est conçu pour travailler comme émetteur dans des équipements comportant une boucle de courant 20 mA. Traditionnellement, les systèmes à boucle de courant 20 mA signalent un état logique haut en transmettant 20 mA de courant de boucle (SIGNAL) et un état bas en ne laissant pas passer un courant de boucle (ESPACE). Le couplage optique du signal de l'entrée logique à la boucle de courant 20 mA coupe les boucles de masse et garantit une très bonne réjection en mode commun.

L'entrée des données du HCPL-4100 est compatible avec les portes logiques LSTTL, TTL et CMOS. Les circuits intégrés d'entrée pilotent une DEL GaAsP. Le faisceau lumineux émis par la DEL est détecté par un deuxième circuit intégré qui permet le passage de 20 mA avec une fuite de tension inférieure à 2,7 V en l'absence d'émission lumineuse et permet le passage de moins de 2 mA lorsque le faisceau lumineux est présent. La sortie de l'émetteur peut supporter 27 V. Le circuit intégré d'entrée fournit une quantité contrôlée de courant de commande de la DEL tout en tenant compte de la dégradation de la sortie lumineuse de la DEL. Le blindage interne permet de garantir une immunité aux transitoires en mode commun de 1000 Vμs.

Conditions de fonctionnement recommandées

Paramètre	Symbole	Min.	Max.	Unité
Tension d'alimentation	V_{CC}	4,5	20	V
Tension d'entrée basse	V_{IL}	0	0,8	V
Tension d'entrée haute	V_{IH}	2	20	V
Température de fonctionnement	T_A	0	70	°C
Tension de sortie	V_O	0	27	V
Courant de sortie	I_O	0	24	mA

Valeurs limites absolues

(pas de correction jusqu'à 55°C)

Température de stockage . . . . . – 55°C à 125°C
Température de fonctionnement . . . . . – 40°C à 85°C
Température de soudage
des conducteurs . . . . . 260°C pendant 10 s
(1,6 mm au-dessous du plan de base)
Tension d'alimentation - V_O . . . . . 0 à 20 V
Courant moyen à la sortie - I_O . . . . . – 30 mA à 30 mA
Crête du courant de sortie - I_O . . . . . à limitation interne
Tension de sortie - V_O . . . . . – 0,4 V à 27 V
Tension d'entrée - V_I . . . . . – 0,5 V à 20 V
Dissipation à l'entrée - P_I . . . . . 265 mW [1]
Dissipation à la sortie - P_O . . . . . 125 mW [2]
Dissipation totale - P . . . . . 360 mW [3]

Caractéristiques électriques

pour $0°C \leqslant T_A \leqslant 70°C$, $4,5\ V \leqslant V_{CC} \leqslant 20\ V$ sauf indications contraires toutes les valeurs typiques sont portées à $T_A = 25°C$ et $V_{CC} = 5\ V$

Paramètre	Symbole	Min.	Typ.	Max.	Unité	Conditions de mesure		Fig.	Note
Tension de sortie pour l'état signal	V_{MO}		1,8 2,2 2,35	2,25 2,7	V V V	$I_O = 2$ mA $I_O = 12$ mA $I_O = 20$ mA	$V_I = 2$ V	1, 2	
Courant de sortie en court-circuit pour l'état signal	I_{SC}	30	85		mA	$V_I = 2$ V, $V_O = 5$ V à 27 V			4
Courant de sortie pour l'état espace	I_{SO}	0,5	1,1	2	mA	$V_I = 0,8$ V, $V_O = 27$ V		3	
Courant d'entrée niveau bas	I_{IL}		–0,12	–0,32	mA	$V_{CC} = 20$ V, $V_I = 0,4$ V			
Tension d'entrée niveau bas	V_{IL}			0,8	V				
Tension d'entrée niveau haut	V_{IH}	2			V				
Courant d'entrée niveau haut	I_{IH}		 0,005	20 100 250	µA µA µA	$V_I = 2,7$ V $V_I = 5,5$ V $V_I = 20$ V			
Courant d'alimentation	I_{CC}		7 7,8	11,5 13	mA mA	$V_{CC} = 5,5$ V $V_{CC} = 20$ V	$0\ V \leqslant V_I \leqslant 20\ V$		
Isolement entrée/sortie	I_{I-O}*			1	µA	Humidité relative = 45% $T_A = 25°C$, $V_{I-O} = 3000$ Vcc, t = 5 s			5,6
OPT.010	V_{ISO}	2500			V_{EFF}	HR < 50%, t = 1 mn			13
Résistance d'E/S	R_{I-O}		10^{12}		Ω	$V_{I-O} = 500$ Vcc			5
Capacité d'E/S	C_{I-O}		1		pF	f = 1 MHz, $V_{I-O} = 0$ Vcc			5

* Normes JEDEC

Notes :

1. Réduire linéairement au-dessus d'une température de l'air libre de 55°C à raison de 3,8 mW/°C. Une application adéquate des facteurs de réduction évite que la température de jonction du CI dépasse 125°C pour une température ambiante de 85°C.
2. Réduire linéairement au-dessus d'une température de l'air libre de 70°C à raison de 2,3 mW/°C. Une puissance importante peut être dissipée dans le circuit de sortie du HCPL-4100 au cours de la transition de l'état ESPACE à l'état SIGNAL pendant la conduite d'une charge capacitive ou d'une ligne de transmission de données. La dissipation moyenne pendant la transition peut être estimée à l'aide de l'équation suivante qui tient compte d'une charge capacitive : $P = I_{SC}(V_{SO} + V_{MO})/2$. La durée de cette transition peut être estimée à $t = C_{OUT}(V_{SO} - V_{MO})/I_{SC}$. Pour les applications typiques de conduite de paires torsadées de lignes de transmission avec des données NRZ (voir figure 11), la transition représente moins de 10% de la durée d'un bit.
3. Réduire linéairement au-dessus d'une température de l'air libre de 55°C à raison de 5,1 mW/°C.
4. Le courant maximal circulant dans la sortie à l'état SIGNAL (I_{SC}) est limité de façon interne pour protéger le dispositif. La durée du court-circuit de la sortie ne dépasse pas 10 ms.
5. Le dispositif est considéré comme une unité à deux bornes, les broches 1, 2, 3 et 4 étant reliées ensemble et les broches 5, 6, 7 et 8 étant aussi reliées ensemble.
6. Cette spécification est également validée par l'application de 2500 Vca pendant 1 s.

HEWLETT PACKARD

COMPOSANTS

RECEPTEUR A BOUCLE DE COURANT 20 mA A COUPLAGE OPTIQUE

HCPL-4200

FICHE TECHNIQUE JANVIER 1986

SCHEMA

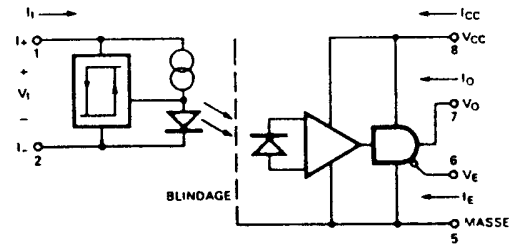
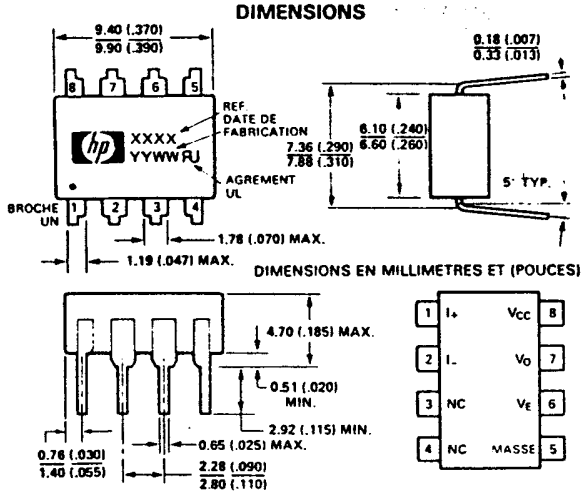


TABLE DE VERITE
(Logique positive)*

I_f	V_E	V_O
H	H	Z
L	H	Z
H	L	H
L	L	L

* CONVENTION DE LA BOUCLE DE COURANT – H = SIGNAL I_f = 12 mA, L = ESPACE I_f = 3 mA, Z = HORS SERVICE (HAUTE IMPEDANCE)

DIMENSIONS



DIMENSIONS EN MILLIMETRES ET (POUCES)

Caractéristiques

- **SORTIE DES DONNEES COMPATIBLE LSTTL, TTL ET CMOS**
- **VITESSE DE TRANSMISSION : 20 KBauds SUR UNE LIGNE DE 1400 m**
- **PERFORMANCES GARANTIES ENTRE 0 ET 70°C**
- **SEUILS EN/HORS GARANTIS**
- **DEL PROTEGEE DES SURINTENSITES**
- **HYSTERESIS DE SEUIL A L'ENTREE**
- **SORTIE TROIS ETATS COMPATIBLE AVEC LES BUS DE TRANSMISSION DE DONNEES**
- **BLINDAGE INTERNE FAVORISANT UNE TRES BONNE REJECTION EN MODE COMMUN**
- **AGREMENT UL (DOSSIER N° E55361) POUR UNE TENSION D'ISOLEMENT TESTEE A 1440 Vca PENDANT 1 mn ET 2500 Vca PENDANT 1 mn (OPTION 010)**
- **EGALEMENT DISPONIBLE : HCPL-4100, EMETTEUR A BOUCLE DE COURANT 20 mA A COUPLAGE OPTIQUE**

Applications

- **MISE EN ŒUVRE D'UN RECEPTEUR ISOLE A BOUCLE DE COURANT 20 mA DANS :**
  les périphériques de systèmes informatiques
  l'équipement industriel de commande
  l'équipement de transmission de données

Description

Le photocoupleur HCPL-4200 est conçu pour travailler comme récepteur dans des équipements comportant une boucle de courant 20 mA. Traditionnellement, les systèmes à boucle de courant 20 mA signalent un état logique haut en transmettant 20 mA de courant de boucle (SIGNAL) et un état bas en ne laissant pas passer un courant de boucle (ESPACE) dépassant quelques milliampères. Le couplage optique du signal de la boucle de courant 20 mA à la sortie logique interrompt les boucles de masse et garantit une très bonne réjection en mode commun. Le HCPL-4200 facilite le processus de conception en permettant au technicien de disposer de seuils garantis pour les états logiques hauts et logiques bas pour la boucle de courant, constituant une interface logique compatible LSTTL, TTL ou CMOS et assurant une bonne réjection en mode commun. Le circuit tampon du côté boucle de courant du HCPL-4200 fournit typiquement un hystérésis de 0,8 mA qui accroît l'immunité aux bruits en mode commun et en mode différentiel. Le tampon fournit également une quantité contrôlée de courant de commande de la DEL tout en tenant compte de la dégradation de la sortie lumineuse de la DEL. Le blindage interne permet de garantir une immunité aux transitoires en mode commun de 1000 V/µs.

Conditions de fonctionnement recommandées

Paramètre	Symbole	Min.	Max.	Unité
Tension d'alimentation	V_{CC}	4,5	20	V
Courant direct à l'entrée (ESPACE)	I_{SI}	0	2	mA
Courant direct à l'entrée (SIGNAL)	I_{MI}	14	24	mA
Température de fonctionne[t]	T_A	0	70	°C
Sortance	N	0	4	Charge TTL
Tension de validation logique bas	V_{EL}	0	0,8	V
Tension de validation logique haut	V_{EH}	2	20	V

Valeurs limites absolues

(pas de correction jusqu'à 70°C)

Température de stockage . . . . . − 55°C à + 125°C
Température de fonctionnement . . . . . − 40°C à + 85°C
Température de soudage . . . . . 260°C pendant 10 s
(1,6 mm en dessous du plan d'assise)
Tension d'alimentation, V_{CC} . . . . . 0 V à 20 V
Courant moyen à l'entrée, I_I . . . . . − 30 mA à + 30 mA
Crête de transitoire de courant à l'entrée, I_I . . . . . 0,5 A[1]
Tension de validation à l'entrée, V_E . . . . . − 0,5 V à + 20 V
Tension de sortie, V_O . . . . . − 0,5 V à + 20 V
Courant moyen de sortie, I_O . . . . . 25 mA
Dissipation à l'entrée, P_I . . . . . 90 mW[2]
Dissipation en sortie, P_O . . . . . 210 mW[3]
Dissipation, P . . . . . 255 mW[4]

Caractéristiques électriques

Pour 0°C ≤ T_A ≤ 70°C; 4,5 V ≤ V_{CC} ≤ 20 V; V_E = 0,8 V;
sauf indication contraire, toutes les valeurs sont typiques dans les conditions suivantes : T_A = 25°C; V_{CC} = 5 V.

Paramètre	Symbole	Min.	Typ.	Max.	Unité	Conditions de mesure		Figure	Note
Courant d'entrée pour l'état signal	I_{MI}	12			mA			1, 2, 3	
Tension d'entrée pour l'état signal	V_{MI}		2,52	2,75	V	I_I = 20 mA	V_E = Indifférent	3, 4	
Courant d'entrée pour l'état espace	I_{SI}			3	mA			1, 2, 3	
Tension d'entrée pour l'état espace	V_{SI}		1,6	2,2	V	I_I = 0,5 à 2 mA	V_E = Indifférent	1, 3	
Courant d'hystérésis à l'entrée	I_{HYS}	0,3	0,6		mA			1	
Tension de sortie logique basse	V_{OL}			0,5	V	I_{OL}= 6,4mA (4 portes TTL), I_I = 3mA		5	
Tension de sortie logique haute	V_{OH}	2,4			V	I_{OH} = 2,6 mA	I_F = 12 mA	6	
Courant de fuite en sortie ($V_{OUT} > V_{CC}$)	I_{OHH}			100	µA	V_O = 5,5 V	I_I = 20 mA, V_{CC} = 4,5 V		
				500	µA	V_O = 20 V			
Tension de validation logique haut	V_{EH}	2			V				
Tension de validation logique bas	V_{EL}			0,8	V				
Courant de validation logique haut	I_{EH}			20	µA	V_E = 2,7 V			
				100	µA	V_E = 5,5 V			
			0,004	250	µA	V_E = 20 V			
Courant de validation logique bas	I_{EL}			−0,32	mA	V_E = 0,4 V			
Courant d'alimentation logique bas	I_{CCL}		4,5	6	mA	V_{CC} = 5,5 V	I_I = 0 mA, V_E = Indifférent		
			5,25	7,5	mA	V_{CC} = 20 V			
Courant d'alimentation logique haut	I_{CCH}		2,7	4,5	mA	V_{CC} = 5,5	I_I = 20 mA, V_E = Indifférent		
			3,1	6	mA	V_{CC} = 20 V			
Courant de sortie état haute impédance	I_{OZL}			−20	µA	V_O = 0,4 V	V_E=2V, I_I=20mA		
	I_{OZH}			20	µA	V_O = 2,4 V	V_E = 2 V, I_I = 0 mA		
				100	µA	V_O = 5,5 V			
				500	µA	V_O = 20 V			
Courant de sortie logique bas en court circuit	I_{OSL}	25			mA	V_O = V_{CC} = 5,5V	I_I = 0 mA		
		40			mA	V_O = V_{CC} = 20V			5
Courant de sortie logique haut en court circuit	I_{OSH}	−10			mA	V_{CC} = 5,5 V	I_I = 20 mA, V_O = Masse		5
		−25			mA	V_{CC} = 20 V			
Isolement d'entrée/sortie	I_{I-O}*			1	µA	Humidité relative = 45%, t = 5 s, V_{I-O} = 3 kVcc, T_A = 25°C			6, 7
OPT 010	V_{ISO}	2500			V_{EFF}	Humidité relative ≤50%, t = 1 mn			14
Résistance d'entrée/sortie	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vcc			6
Capacité d'entrée/sortie	C_{I-O}		1		pF	f = 1 MHz, V_{I-O} = 0 Vcc			6
Capacité d'entrée	C_{IN}		120		pF	f = 1 MHz, V_I = 0 Vcc, broches 1 et 2			

* Normes JEDEC

ANALOG DEVICES

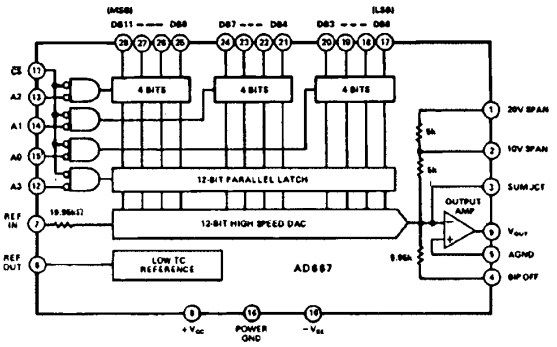
Microprocessor-Compatible 12-Bit D/A Converter

AD667*

FEATURES

- Complete 12-Bit D/A Function
  - Double-Buffered Latch
  - On Chip Output Amplifier
  - High Stability Buried Zener Reference
- Single Chip Construction
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2 LSB max
- Settling Time: 3 µs max to 0.01%
- Guaranteed for Operation with ±12 V or ±15 V Supplies
- Low Power: 300 mW Including Reference
- TTL/5 V CMOS Compatible Logic Inputs
- Low Logic Input Currents
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD667 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin-film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100 ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD667 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD667 is trimmed at the wafer level and is specified to ±1/4 LSB maximum linearity error (K, B grades) at +25°C and ±1/2 LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity, is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD667 is thus well suited for wide temperature range performance with ±1/2 LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain TC is 5 ppm/°C.

*Protected by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.

REV. A

The AD667 is available in five performance grades. The AD667J and K are specified for use over the 0°C to +70°C temperature range and are available in a 28-pin molded plastic DIP (N) or PLCC (P) package. The AD667S grade is specified for the -55°C to +125°C range and is available in the ceramic DIP (D) or LCC (E) package. The AD667A and B are specified for use over the -25°C to +85°C temperature range and are available in a 28-pin hermetically sealed ceramic DIP (D) package.

PRODUCT HIGHLIGHTS

1. The AD667 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried Zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.
5. The precision high speed current steering switch and on-board high speed output amplifier settle within 1/2 LSB for a 10 V full-scale transition in 2.0µs as when properly compensated.
6. The AD667 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD667/883B data sheet for detailed specifications.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD667–SPECIFICATIONS (@ T_A = +25°C, ± 12 V, ± 15 V power supplies unless otherwise noted)

Model	AD667J Min	AD667J Typ	AD667J Max	AD667K Min	AD667K Typ	AD667K Max	Units
DIGITAL INPUTS							
Resolution			12			12	Bits
Logic Levels (TTL, Compatible, T_{MIN}-T_{MAX})[1]							
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5 V)		3	10		3	10	µA
I_{IL} (V_{IL} = 0.8 V)		1	5		1	5	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_A = T_{MIN} to T_{MAX}		Monotonicity Guaranteed			Monotonicity Guaranteed		LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	% FSR[3]
Unipolar Offset Error[2]		±1	±2		±1	±2	LSB
Bipolar Zero[2]		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT							
Differential Linearity		±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{MIN} or T_{MAX}		±5	±30		±5	±15	ppm of FSR/°C
Unipolar Offset T_A = -25°C to T_{MIN} or T_{MAX}		±1	±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{MIN} or T_{MAX}		±5	±10			±10	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2 kΩ ‖500 pF Load)							
with 10 kΩ Feedback		3	4		3	4	µs
with 5 kΩ Feedback		2	3		2	3	µs
For LSB Change		1			1		µs
Slew Rate	10			10			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			mA
Output Impedance (DC)		0.05			0.05		Ω
Short Circuit Current			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 V to +16.5 V dc		5	10		5	10	ppm of FS/%
V_{EE} = -11.4 V to -16.5 V dc		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			±12, ±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	V
Supply Current							
+11.4 V to +16.5 V dc		8	12		8	12	mA
-11.4 V to -16.5 V dc		20	25		20	25	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	-65		+125	-65		+125	°C

NOTES

[1]The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.

[2]Adjustable to zero.

[3]FSR means "Full-Scale Range" and is 20 V for ±10 V range and 10 V for the ±5 V range.

[4]A minimum power supply of ±12.5 V is required for a ±10 V full-scale output and ±11.4 V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TIMING SPECIFICATIONS

(All Models, T_A = +25°C, V_{CC} = +12 V or +15 V, V_{EE} = -12 V or -15 V)

Symbol	Parameter	Min	Typ	Max	
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

ABSOLUTE MAXIMUM RATINGS

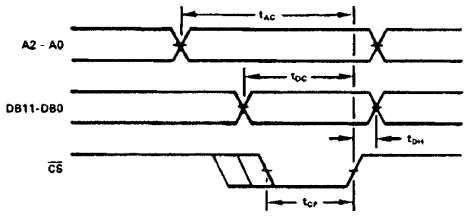
V_{CC} to Power Ground ..... 0 V to +18 V
V_{EE} to Power Ground ..... 0 V to -18 V
Digital Inputs (Pins 11-15, 17-28)
to Power Ground ..... -1.0 V to +7.0 V
Ref In to Reference Ground ..... ±12 V
Bipolar Offset to Reference Ground ..... ±12 V
10 V Span R to Reference Ground ..... ±12 V
20 V Span R to Reference Ground ..... ±24 V
Ref Out, V_{OUT} (Pins 6, 9) .. Indefinite Short to Power Ground
..... Momentary Short to V_{CC}
Power Dissipation ..... 1000 mW

Model	AD667A			AD667B			AD667S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIGITAL INPUTS										
Resolution			12			12			12	Bits
Logic Levels (TTL, Compatible, T_{MIN}–T_{MAX})[1]										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.7	V
I_{IH} (V_{IH} = 5.5 V)		3	10		3	10		3	10	μA
I_{IL} (V_{IL} = 0.8 V)		1	5		1	5		1	5	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4		±1/8	±1/2	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2		±1/8	±3/4	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2		±1/4	±3/4	LSB
T_A = T_{MIN} to T_{MAX}	Monotonicity Guaranteed			Monotonicity Guaranteed			Monotonicity Guaranteed			LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	% FSR[3]
Unipolar Offset Error[2]		±1	±2		±1	±2		±1	±2	LSB
Bipolar Zero[2]		±0.05	±0.1		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT										
Differential Linearity		±2			±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{MIN} or T_{MAX}		±5	±30		±5	±15		±15	±30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{MIN} or T_{MAX}		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{MIN} or T_{MAX}		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ±0.01% of FSR for										
FSR Change (2 kΩ ‖500 pF Load)										
with 10 kΩ Feedback		3	4		3	4		3	4	μs
with 5 kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (DC)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		1.0			mA
POWER SUPPLY SENSITIVITY										
V_{CC} = +11.4 V to +16.5 V dc		5	10		5	10		5	10	ppm of FS/%
V_{EE} = –11.4 V to –16.5 V dc		5	10		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±12, ±15			±12, ±15			±12, ±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	±11.4		±16.5	V
Supply Current										
+11.4 V to +16.5 V dc		8	12		8	12		8	12	mA
–11.4 V to –16.5 V dc		20	25		20	25		20	25	mA
TEMPERATURE RANGE										
Specification	–25		+85	–25		+85	–55		+125	°C
Storage	–65		+150	–65		+150	–65		+150	°C

TIMING DIAGRAMS

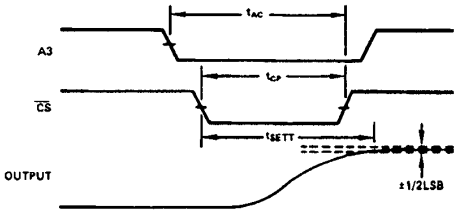
WRITE CYCLE #1

(Load First Rank from Data Bus; A3 = 1)



WRITE CYCLE #2

(Load Second Rank from First Rank; A2, A1, A0 = 1)



Tournez la page S.V.P.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD667 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5 V or unipolar output voltage ranges of 0 V to +5 V or 0 V to +10 V.

Gain and offset drift are minimized in the AD667 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table I.

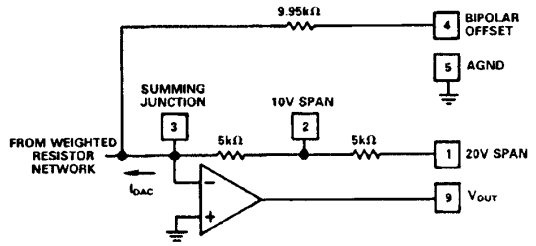


Figure 1. Output Amplifier Voltage Range Scaling Circuit

UNIPOLAR CONFIGURATION (Figure 2)

This configuration will provide a unipolar 0 volt to +10 volt output range. In this mode, the bipolar offset terminal, Pin 4, should be grounded if not used for trimming.

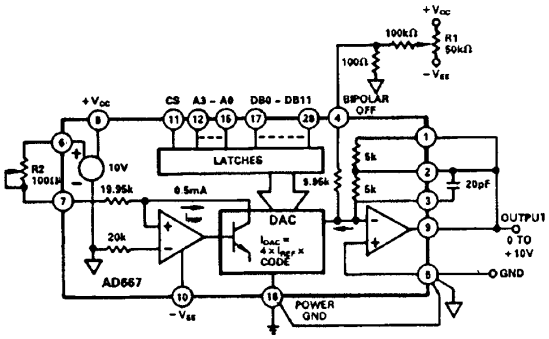


Figure 2. 0 V to +10 V Unipolar Voltage Output

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1 LSB = 2.44 mV). In most cases this trim is not needed, and Pin 4 should be connected to Pin 5.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100 Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1 LSB less than nominal full scale of 10.000 volts.)

BIPOLAR CONFIGURATION (Figure 3)

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1s).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100 Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100 Ω gain trimmer R2 to give a reading of +4.9976 volts.

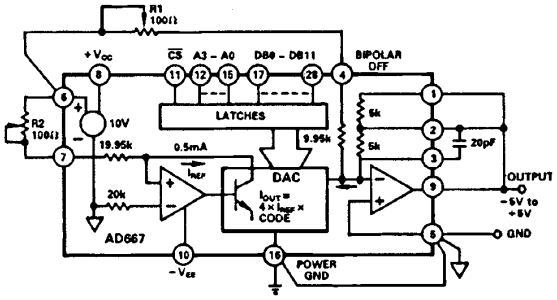


Figure 3. ±5 V Bipolar Voltage Output

INTERNAL/EXTERNAL REFERENCE USE

The AD667 has an internal low noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete Zener reference diodes. The performance of the AD667 is specified with the internal reference driving the DAC since all trimming and testing (especially for full-scale error and bipolar offset) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0. 5 mA to Ref In and 1.0 mA to Bipolar Offset). A minimum of 0.1 mA is available for driving external loads. The AD667 reference output should be buffered with an external op amp if it is required to supply more than 0.1 mA output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full-scale TC for a particular grade.

If an external reference is used (10.000 V, for example), additional trim range must be provided, since the internal reference has a tolerance of ±1%, and the AD667 full-scale and bipolar offset are both trimmed with the internal reference. The gain and offset trim resistors give about ±0.25% adjustment range, which is sufficient for the AD667 when used with the internal reference.

It is also possible to use external references other than 10 volts. The recommended range of reference voltage is from +8 to +11 volts, which allows both 8.192 V and 10.24 V ranges to be used. The AD667 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range in a particular application, a CMOS multiplying DAC is a better choice.

Reduced values of reference voltage will also permit the ±12 volt ± 5% power supply requirement to be relaxed to ±12 volts ± 10%.

It is not recommended that the AD667 be used with external feedback resistors to modify the scale factor. The internal resistors are trimmed to ratio-match and temperature-track the other resistors on the chip, even though their absolute tolerances are ±20%, and absolute temperature coefficients are approximately -50 ppm/°C. If external resistors are used, a wide trim range (±20%) will be needed and temperature drift will be increased to reflect the mismatch between the temperature coefficients of the internal and external resistors.

Tournez la page S.V.P.

AD667

Small resistors may be added to the feedback resistors in order to accomplish small modifications in the scaling. For example, if a 10.24 V full scale is desired, a 140 Ω 1% low TC metal-film resistor can be added in series with the internal (nominal) 5k feedback resistor, and the gain trim potentiometer (between Pins 6 and 7) should be increased to 200 Ω. In the bipolar mode, increase the value of the bipolar offset trim potentiometer also to 200 Ω.

GROUNDING RULES

The AD667 brings out separate analog and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low level signal paths.

The analog ground at Pin 5 is the ground point for the output amplifier and is thus the "high quality" ground for the AD667; it should be connected directly to the analog reference point of the system. The power ground at Pin 16 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200 mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

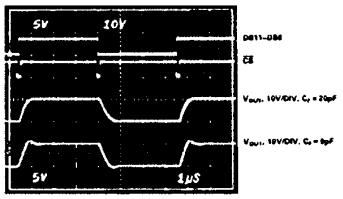
It is also important to apply decoupling capacitors properly on the power supplies for the AD667 and the output amplifier. The correct method for decoupling is to connect a capacitor from each power supply pin of the AD667 to the analog ground pin of the AD667. Any load driven by the output amplifier should also be referred to the analog ground pin.

OPTIMIZING SETTLING TIME

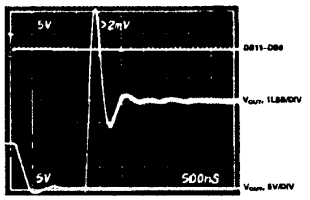
The dynamic performance of the AD667's output amplifier can be optimized by adding a small (20 pF) capacitor across the feedback resistor. Figure 4 shows the improvement in both large-signal and small-signal settling for the 10 V range. In Figure 4a, the top trace shows the data inputs (DB11-DB0 tied together), the second trace shows the CS pulse (A3-A0 tied low), and the lower two traces show the analog outputs for C_F = 0 pF and 20 pF respectively.

Figures 4b and 4c show the settling time for the transition from all bits on to all bits off. Note that the settling time to ± 1/2 LSB for the 10 V step is improved from 2.4 microseconds to 1.6 microseconds by the addition of the 20 pF capacitor.

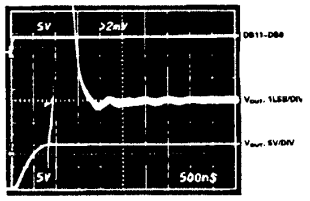
Figures 4d and 4e show the settling time for the transition from all bits off to all bits on. The improvement in settling time gained by adding C_C = 20 pF is similar.



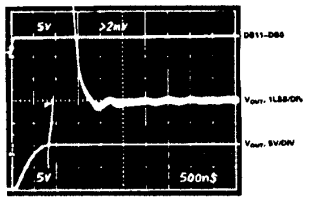
a. Large Scale Settling



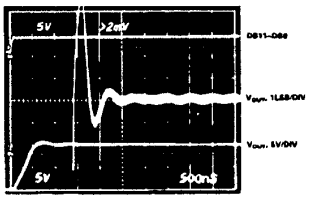
b. Fine-Scale Settling, C_F = 0 pF



c. Fine-Scale Settling, C_F = 20 pF



d. Fine-Scale Settling, C_F = 0 pF



e. Fine-Scale Settling, C_F = 20 pF

Figure 4. Settling Time Performance

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD667 consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers which can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 5 shows the block diagram of the AD667 logic section.

The latches are controlled by the address inputs, A0-A3, and the $\overline{CS}$ input. All control inputs are active low, consistent with general practice in microprocessor systems. The four address lines each enable one of the four latches, as indicated in Table II.

All latches in the AD667 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. When any one of the control signals returns high, the data is latched.

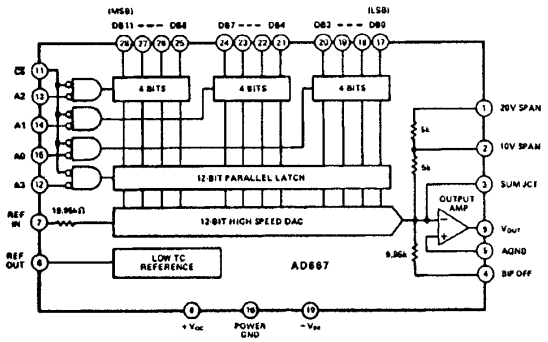


Figure 5. AD667 Block Diagram

It is permissible to enable more than one of the latches simultaneously. If a first rank latch is enabled coincident with the second rank latch, the data will reach the second rank correctly if the "WRITE CYCLE #1" timing specifications are met.

Table II. AD667 Truth Table

$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

INPUT CODING

The AD667 uses positive-true binary input coding. Logic "1" is represented by an input voltage greater than 2.0 V and Logic "0" is defined as an input voltage less than 0.8 V.

Unipolar coding is straight binary, where all zeroes (000_H) on the data inputs yields a zero analog output and all ones (FFF_H) yields an analog output 1 LSB below full scale.

Bipolar coding is offset binary, where an input code of 000_H yields a minus full-scale output, an input of FFF_H yields an output 1 LSB below positive full scale, and zero occurs for an input code with only the MSB on (800_H).

The AD667 can be used with twos complement input coding if an inverter is used on the MSB (DB11).

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can thus interface with any type of 5 volt logic. The configuration of the input circuit is shown in Figure 6.

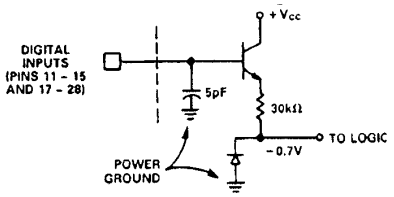


Figure 6. Equivalent Digital Input Circuit

The AD667 data and control inputs will float to a Logic 0 if left open. It is recommended that any unused inputs be connected to power ground to improve noise immunity.

Fanout for the AD667 is 100 when used with a standard low power Schottky gate output device.

8-BIT MICROPROCESSOR INTERFACE

The AD667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats.

Whenever a 12-bit DAC is loaded from an 8-bit bus, two bytes are required. If the program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the 4 most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

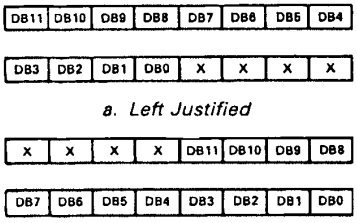


Figure 7. 12-Bit Data Formats for 8-Bit Systems

Figure 8 shows an addressing scheme for use with an AD667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the AD667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

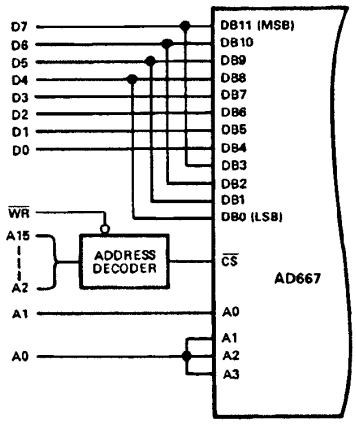


Figure 8. Left-Justified 8-Bit Bus Interface

AD667

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD667 still occupies two adjacent locations in the processor's memory map. In the circuit of Figure 9, location X01 loads the 8 LSBs and location X10 loads the 4 MSBs and updates the output.

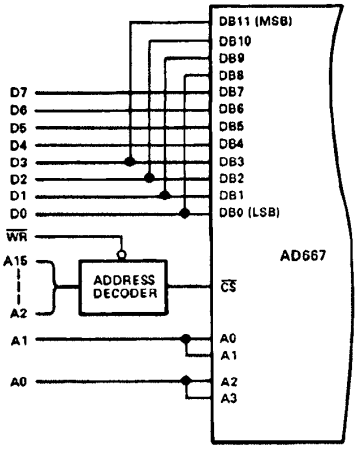


Figure 9. Right-Justified 8-Bit Bus Interface

USING THE AD667 WITH 12- AND 16-BIT BUSES

The AD667 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines (A0 through A3) are tied low, and the latch is enabled by $\overline{CS}$ going low. The AD667 thus occupies a single memory location.

This configuration uses the first and second rank registers simultaneously. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is low will cause activity at the AD667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

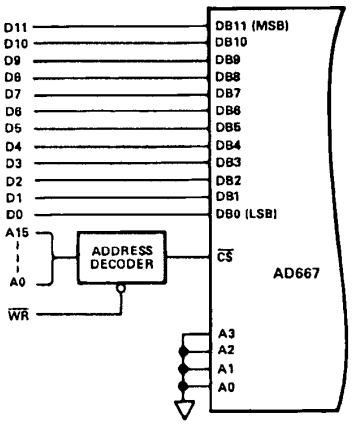


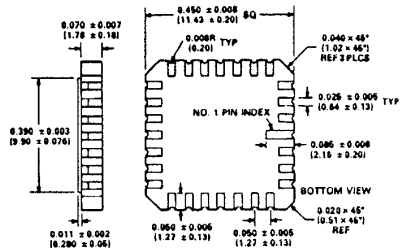
Figure 10. Connections for 12- and 16-Bit Bus Interface

C842b–22–8/87

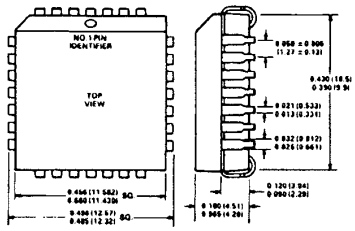
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

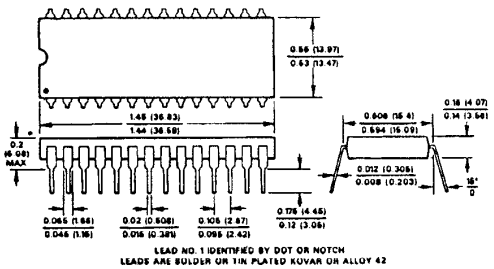
28-Contact LCC (E)



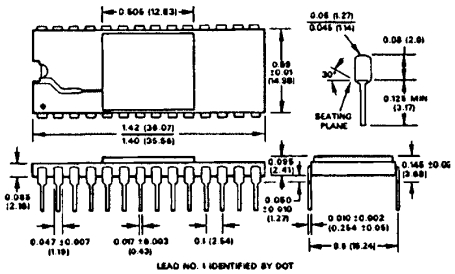
28-Terminal Plastic Leaded Chip Carrier (P)



28-Pin Plastic DIP (N)



28-Pin Ceramic DIP (D)



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National Semiconductor Corporation

PRELIMINAR

LM675 Power Operational Amplifier

General Description

The LM675 is a monolithic power operational amplifier featuring wide bandwidth and low input offset voltage, making it equally suitable for AC and DC applications.

The LM675 is capable of delivering output currents in excess of 3 amps, operating at supply voltages of up to 60V. The device overload protection consists of both internal current limiting and thermal shutdown. The amplifier is also internally compensated for gains of 10 or greater.

Features

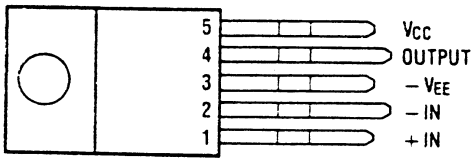
- 3A current capability
- A_{VO} typicaly 90 dB
- 5.5 MHz gain bandwidth product
- 8 V/μs slew rate
- Wide power bandwidth 70 kHz
- 1 mV typical offset voltage
- Short circuit protection
- Thermal protection with parole circuit (100% tested)
- 16V–60V supply range
- Wide common mode range
- internal output protection diodes
- 90 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance power op amp
- Bridge amplifiers
- Motor speed controls
- Servo amplifiers
- Instrument systems

Connection Diagram

TO-220 Power Package (T)

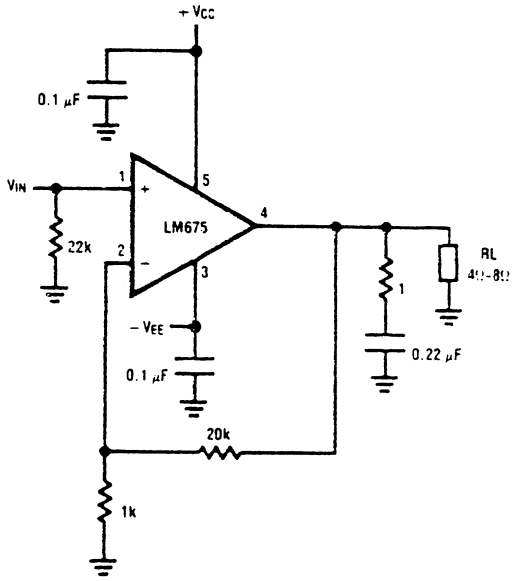


TL/H/6739–1

Front View

Typical Applications

Non-Inverting Amplifier



TL/H/6739

Order Number LM675T
See NS Package T05B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±30V
Input Voltage	$-V_{EE}$ to V_{CC}

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Note 1)	30W
Lead Temperature (Soldering, 10 seconds)	260°C

ESD rating to be determined.

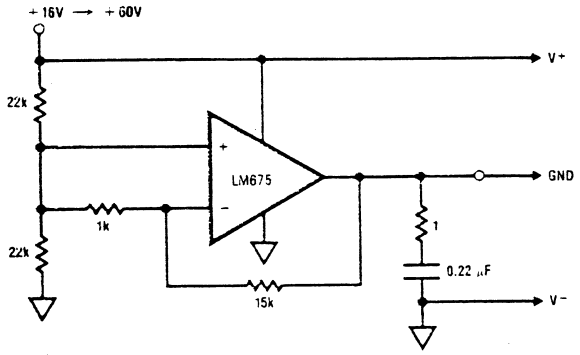
Electrical Characteristics $V_S = \pm 25V$, $T_A = 25°C$ unless otherwise specified.

Parameter	Conditions	Typical	Tested Limit	Units
Supply Current	P_{OUT} = 0W	18	50 (max)	mA
Input Offset Voltage	V_{CM} = 0V	1	10 (max)	mV
Input Bias Current	V_{CM} = 0V	0.2	2 (max)	μA
Input Offset Current	V_{CM} = 0V	50	500 (max)	nA
Open Loop Gain	$R_L = \infty\Omega$	90	70 (min)	dB
PSRR	$\Delta V_S = \pm 5V$	90	70 (min)	dB
CMRR	$V_{IN} = \pm 20V$	90	70 (min)	dB
Output Voltage Swing	$R_L = 8\Omega$	±21	±18 (min)	V
Offset Voltage Drift Versus Temperature	$R_S < 100\ k\Omega$	25		μV/°C
Offset Voltage Drift Versus Output Power		25		μV/W
Output Power	THD = 1%, f_O = 1 kHz, $R_L = 8\Omega$	25	20	W
Gain Bandwidth Product	f_O = 20 kHz, A_{VCL} = 1000	5.5		MHz
Max Slew Rate		8		V/μs
Input Common Mode Range		±22	±20 (min)	V

Note 1: Assumes T_A equal to 70°C. For operation at higher tab temperatures, the LM675 must be derated based on a maximum junction temperature of 150°C.

Typical Applications (Continued)

Generating a Split Supply From a Single Supply



$V_S = \pm 8V \longrightarrow \pm 30V$

TL/H/6739–3

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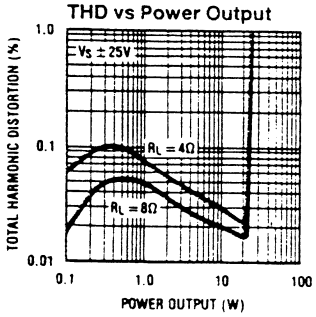
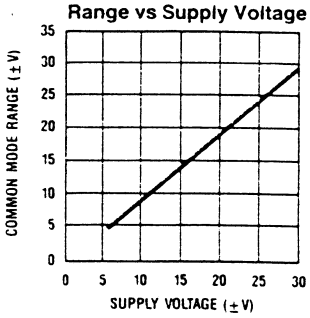
Typical Performance Characteristics

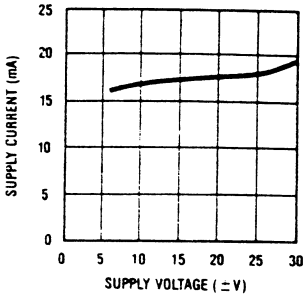
THD vs Power Output



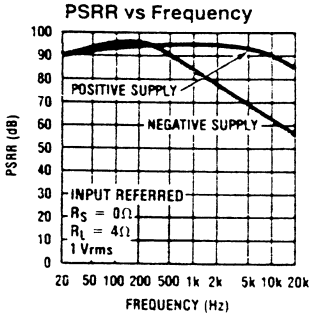
Input Common Mode Range vs Supply Voltage



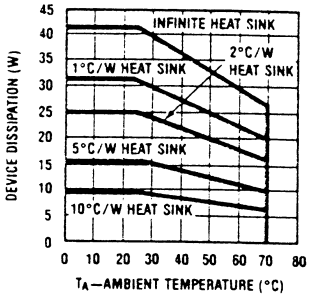
Supply Current vs Supply Voltage



PSRR vs Frequency

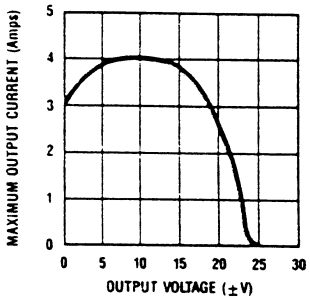


Device Dissipation vs Ambient Temperature†



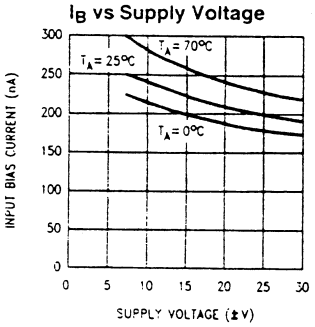
†θ INTERFACE = 1° C/W.
See Application Hints.

Current Limit vs Output Voltage*

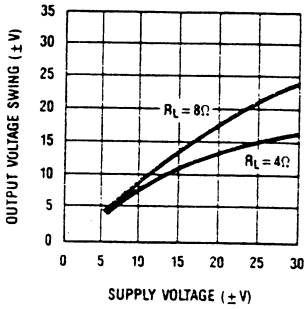


*VS = ±25V

I_B vs Supply Voltage



Output Voltage Swing vs Supply Voltage



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